Verification of Digitally Calibrated Analog Systems with Verilog-AMS Behavioral Models

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Agenda

- Introduction
  - Human Error: Finding and correcting in writing and circuit design
  - How self calibration increases the need for top level simulation and behavioral models
- Block diagram of a representative self-calibrated system
- Categories of design errors
- For each category
  - Example of error
  - Modeling strategy to expose that kind of error
    - Verilog-AMS coding tips
    - How error would be observable
- Conclusion

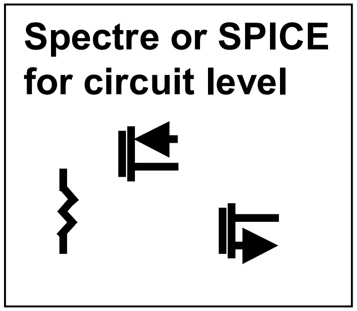
Introduction: Human Error

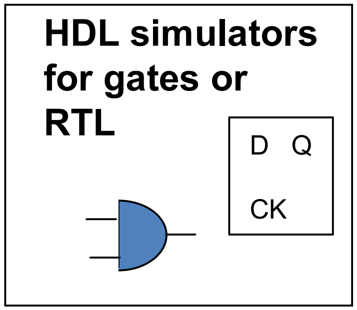
- Original initial sentence of ABSTRACT:
  - This paper describes the use of behavioral models to verify the design of digitally calibrated analog/mixed-signal systems, to large for either a circuit simulator or a traditional digital simulator

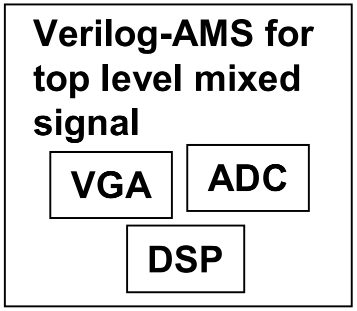
- Reread the previous sentence. Do you see the error?
  - Colin McAndrew, the conference chairman encouraged me to wait till the morning for the final proofreading before submitting the PDF version

Introduction: Human Error

- Apart from innovative ideas and discoveries of applications of physical laws, we must “get it all right” when we build integrated circuits
- Mask sets are expensive and re-spins take weeks or months
- “Getting it right activities” include visually checking schematics and text files, holding design reviews, using design tool audits and of course simulation
- Choose your simulator to fit the task


Spectre or SPICE for circuit level

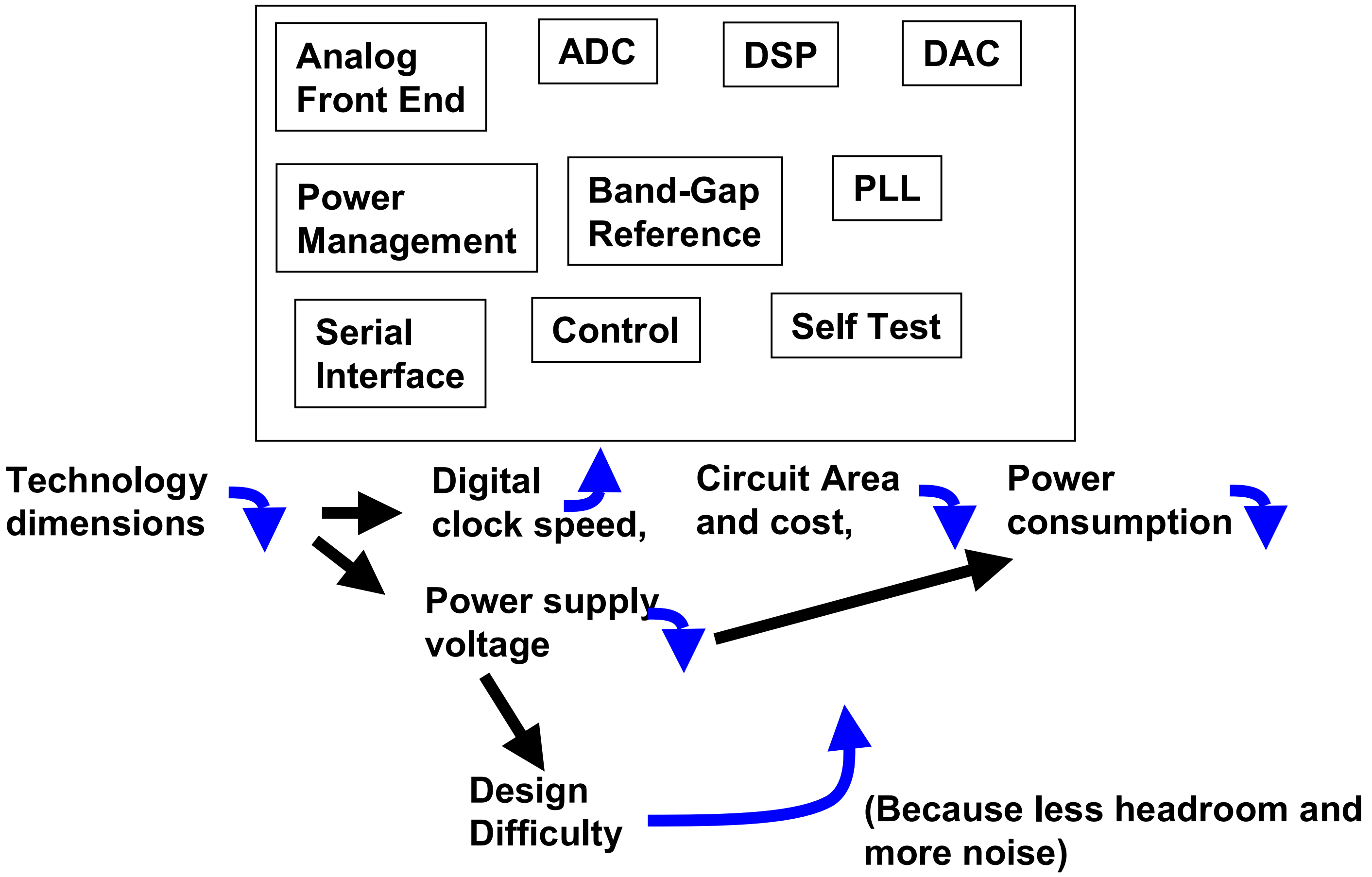

HDL simulators for gates or RTL


Verilog-AMS for top level mixed signal

- Verilog-AMS Simulator is especially useful for final verification

Why Calibration?

- Current trends:
  - Mixed signal integrated circuits – system on a chip. Mostly digital



Analog Front End

ADC

DSP

DAC

Power Management

Band-Gap Reference

PLL

Serial Interface

Control

Self Test

Technology dimensions

Digital clock speed,

Circuit Area and cost,

Power consumption

Power supply voltage

Design Difficulty

(Because less headroom and more noise)

Why Calibration?

- Open loop analog buys back some headroom but you lose the good things that feedback provides

- Here’s how mixed signal calibration stands in for analog feedback
  - Digitize analog quantities (voltages, currents time intervals etc.)
  - Calculate decision criteria from the digital variables
  - Make decisions to vary controlling parameters (currents, voltages, capacitances etc.)
  - Apply the decision by D/A conversion, switches etc.
  - Re-measure and repeat until errors are limited

- Calibrate at start-up and periodically thereafter, to
  - Mitigate offset, gain, frequency, or filter corner frequency errors.
  - Reduce effect of drift with temperature, power supply voltage and aging

- *But now there are lots of new opportunities to make mistakes!*

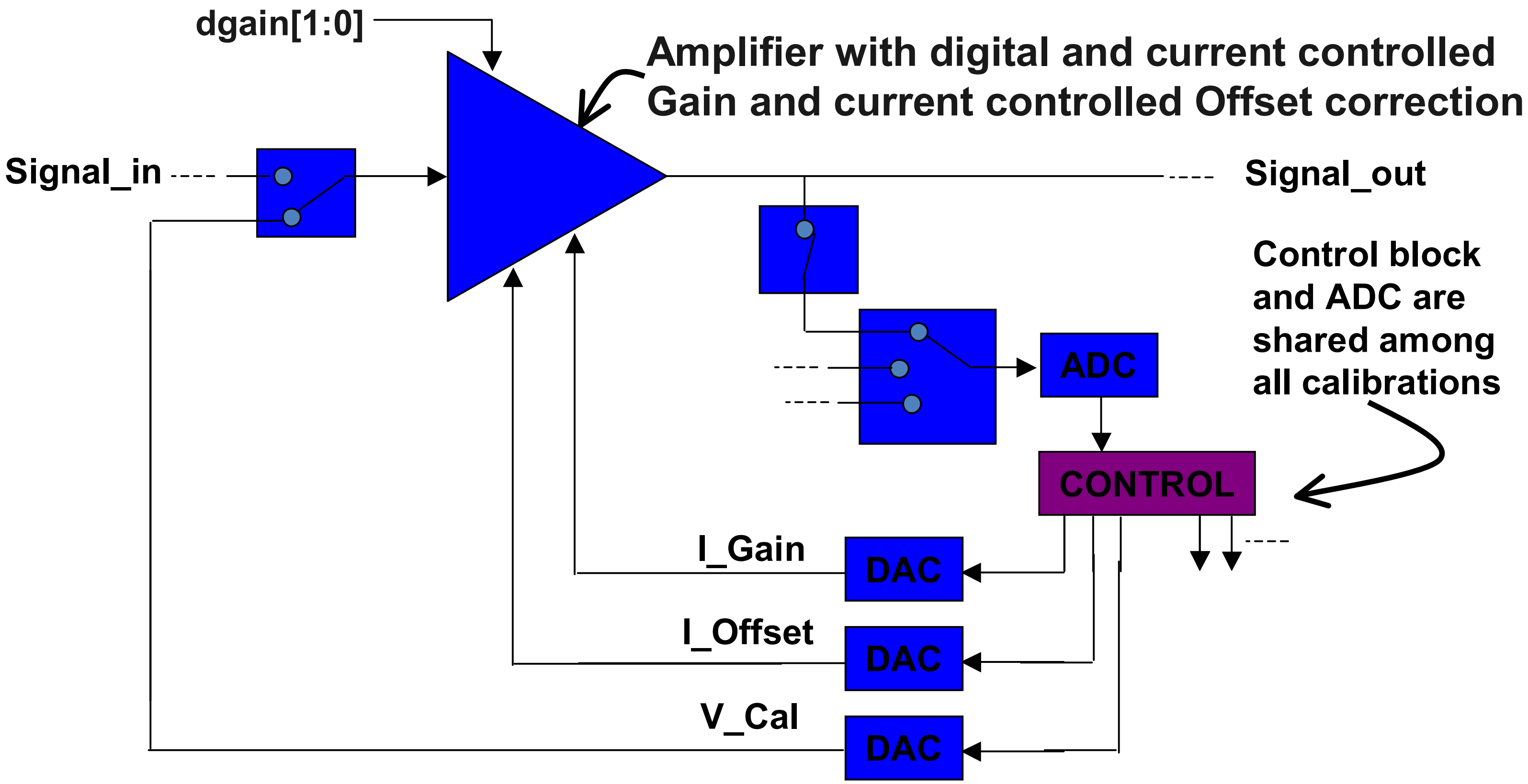
Why Behavioral Models?

- Typical ICs are just too big to fit into a circuit simulator and overlapping partial simulations allow errors to fall through

- Calibration increases the need for top level verification
  - More opportunities for error
    - More inter-block communication
    - More collaboration between designers
    - More analog/digital interfaces

- Behavioral models are a powerful, flexible tool which enables simulating an IC from the top level

Representative Block Diagram



Amplifier with digital and current controlled Gain and current controlled Offset correction

Control block and ADC are shared among all calibrations

Analog / Mixed Signal

Digital

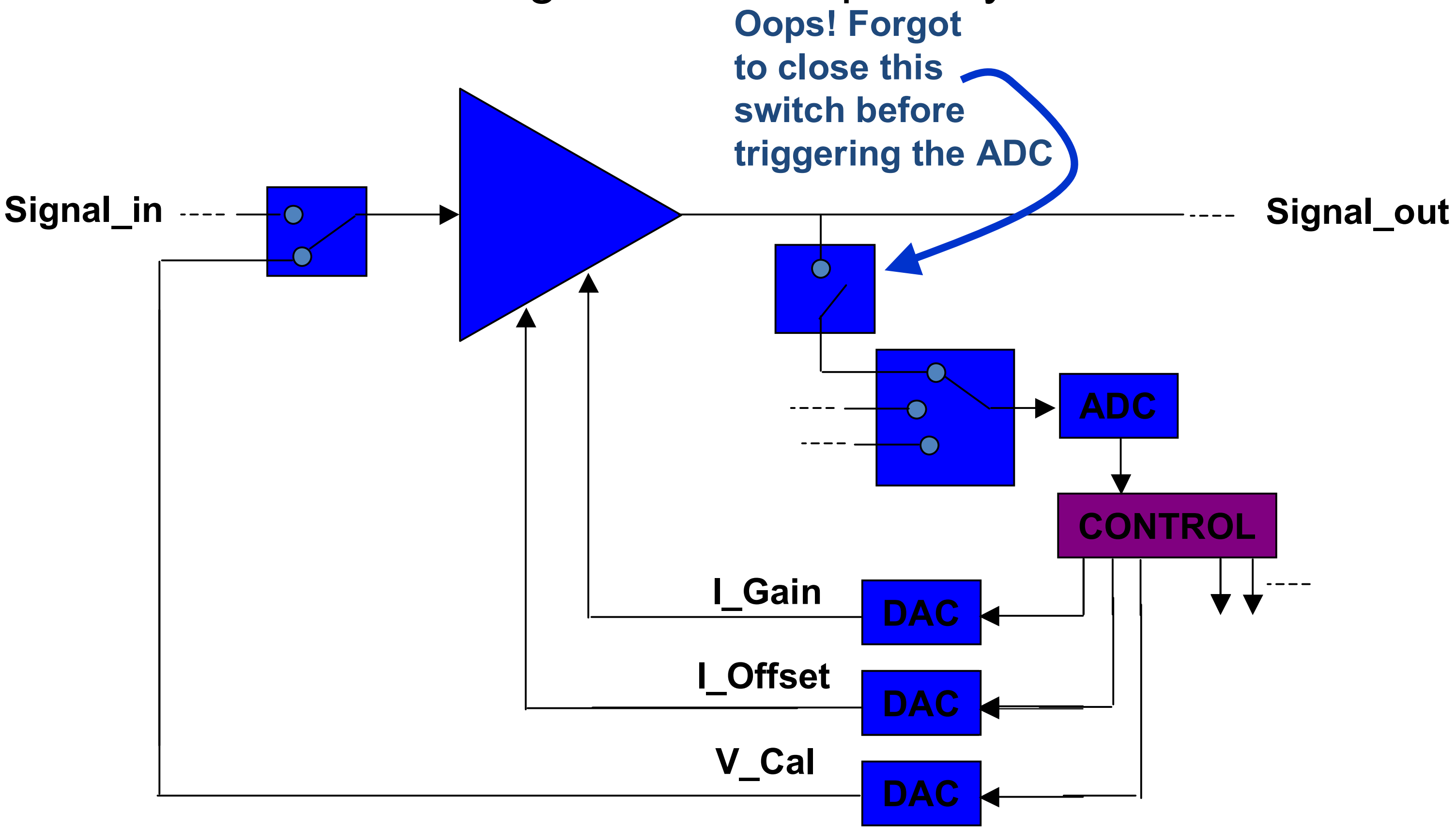
Categories of Design Errors

1. Faulty Calibration Algorithm
2. Bus Bit Order Errors
3. Digital Control Polarity Errors
4. Digital Signal Integrity Errors
5. Bias Current Errors
   1. Polarity
   2. Multiple Sinks
6. Reference Voltage Errors
   1. Choosing Wrong Voltage Reference
   2. Resistively Loading High Impedance Reference

- What other ways can we screw things up?

1. Faulty calibration algorithm

- Semantic errors such as forgetting to close a switch or to power up
- Semantic errors resulting in reversed polarity of correction



Oops! Forgot to close this switch before triggering the ADC

Catching Algorithmic Errors

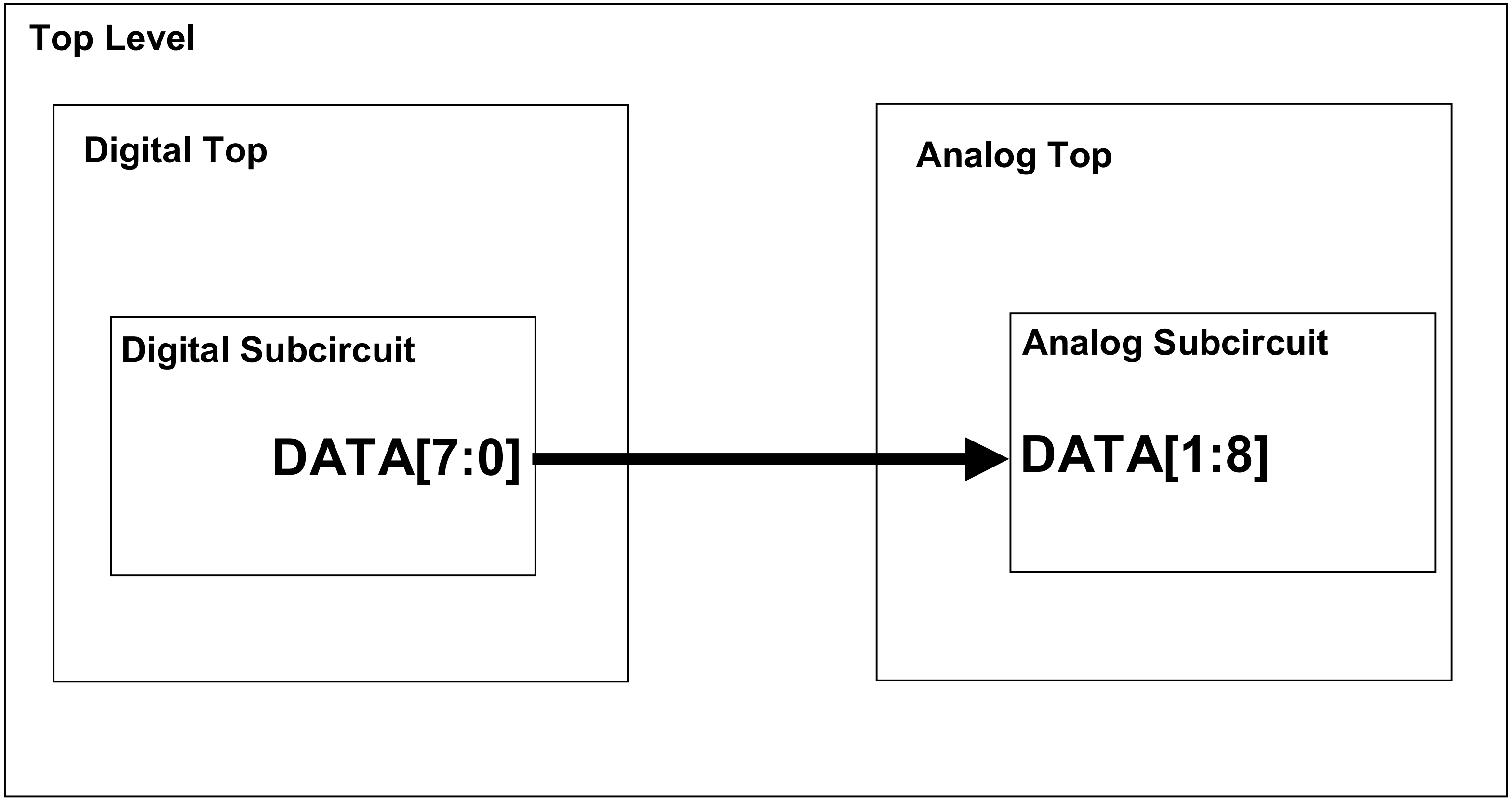
- Good behavioral modeling techniques:
  - Monitor power supplies, bias currents and reference voltages. Display error message and disable model operation if out of limits
  - React properly to all controlling inputs such as power-down (or enable), and controls for gain, polarity etc.
  - Pessimistically model power-up timing limits. If there's a spec for the maximum time interval between a block's power-up and its normal operation, write the model to have no output until that time interval has passed

- Verilog AMS tip:
  - Use transition() statements in the analog section of the model
    - To trigger an analog solution from a digital input transition create an interim real variable in the digital section which responds stepwise to digital stimulus. Make the electrical variable (or another real variable) in the analog section becomes a transition() of the stepwise variable
      - transition() forces analog solution points when the stepwise variable changes
      - transition() eliminates the first order discontinuity of the signal step which could cause loss of convergence

- For the algorithmic error illustrated on the previous page:
  - The control loop will not close because the amplifier output is not observed. The consequences are observable in waveforms. CONTROL may be designed to detect and flag the lack of response

2. Bus Bit Order Errors

- Digital designer produces DATA[7:0]
- Analog designer expects DATA[1:8]



- **Have you seen this kind of miscommunication escape review?**

Catching Bit-Order Errors

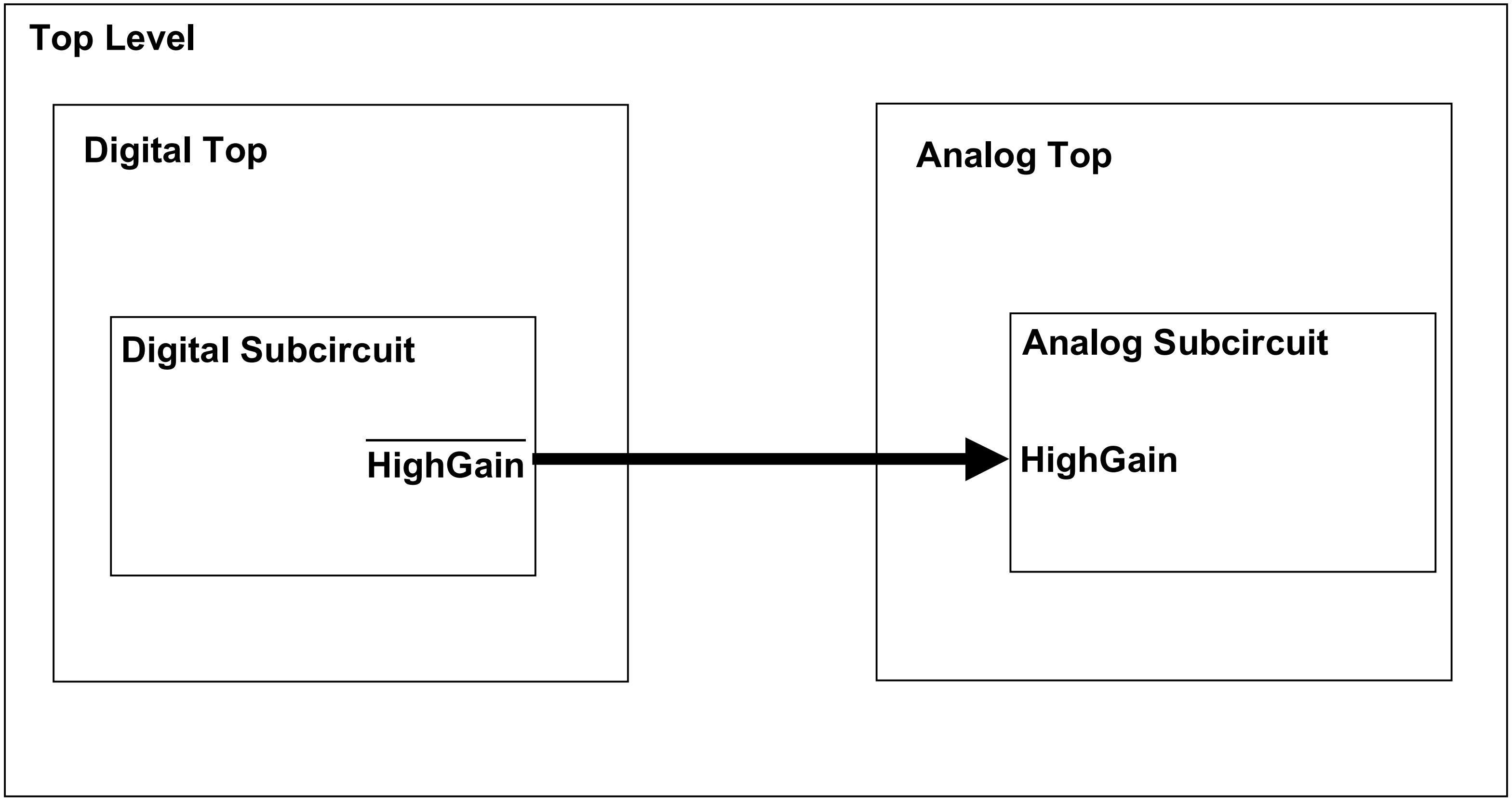
- Good behavioral modeling technique:
  - Write models to “blindly” respond to actual inputs – making no assumptions about expected inputs

- Verilog AMS tip:
  - Make sure the model can respond to every possible input combination
    - Use case statements for all legitimate input combinations
    - All other combinations fall into the “default” statement, resulting in error messages and output shut down

- For the bit-order error illustrated on the previous page:
  - The amplifier output won’t change as expected because of the bit reversal, so the control loop will not close. The consequences are observable in waveforms. CONTROL may be designed to detect and flag the lack of response

3. Digital Control Polarity Errors

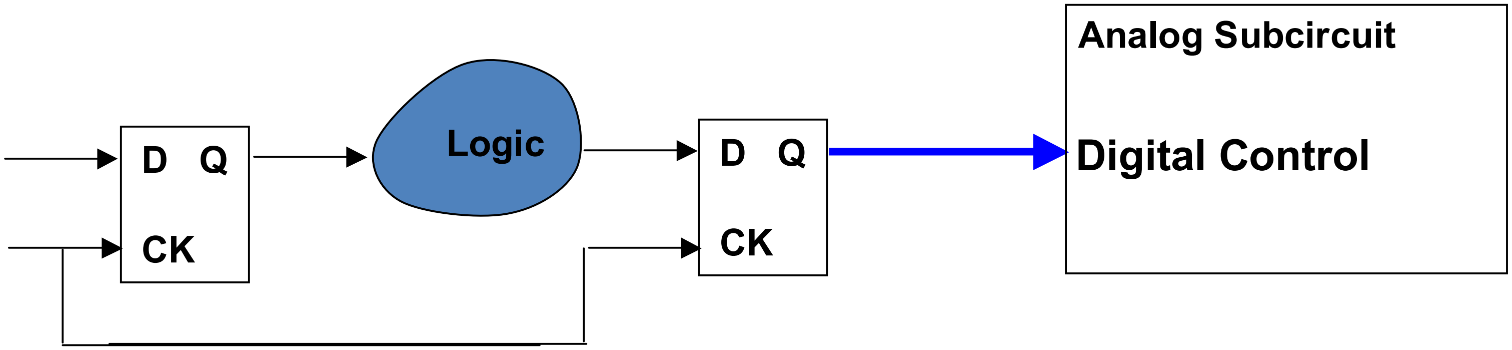
- Digital designer produces active low option control
- Analog designer expects active high option control



- **Have you seen this error? How about power down versus enable?**

4. Digital Signal Integrity Errors

- Setup and hold faults are more likely to escape detection in schematic-based digital circuits created by analog designers



- These faults can be a nightmare to debug in the laboratory or in the field
  - May depend on processing, power supply voltage, temperature (PVT)

Catching Digital Signal Integrity Errors

- Good behavioral modeling technique: Don’t assume that if it isn’t a one, it’s a zero!
  - if (“1”) …
  - else if (“0”) …
  - else … (respond to error)

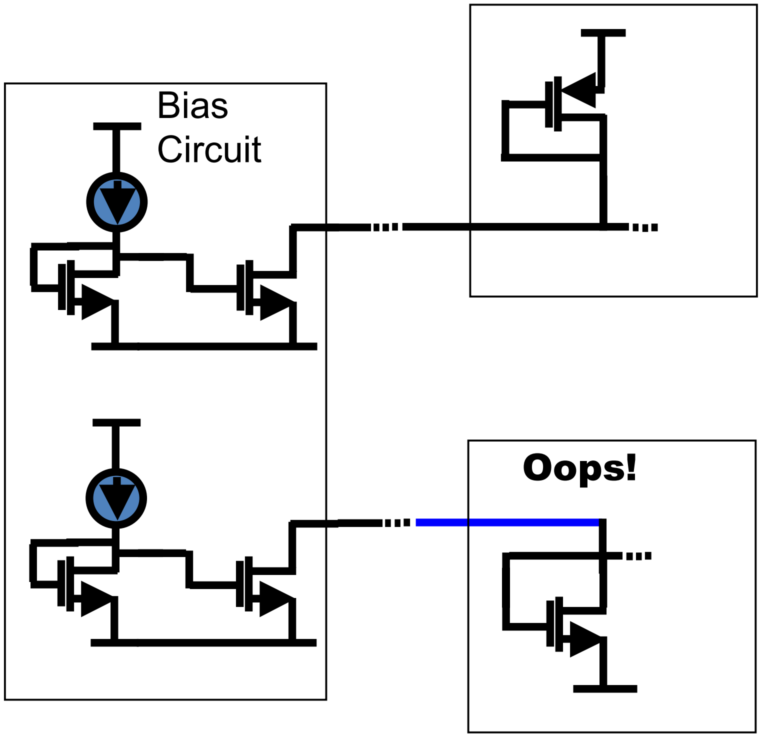
- Verilog AMS tip:
  - Make it easier to debug problems by using informative display statements:
    - Use %m to indicate hierarchically the module which is receiving bad input
    - Use %g to indicate the time of the error
    - Displaying the variable value is helpful when it is more than one bit wide

```
$display(
  "ERROR : %g : %m : Illegal value: sel = %2b ",
$realtime, sel);
```

  - Simulate digital circuitry at the gate level using extracted parasitics, enabling timing audits
- For the Q = “X” error on the previous page:
  - The analog module receiving digital input Q will display a message stating the time, the path to itself and the value of Q. Also, the analog module output shuts down, making the error difficult to ignore

5. Bias Current Errors

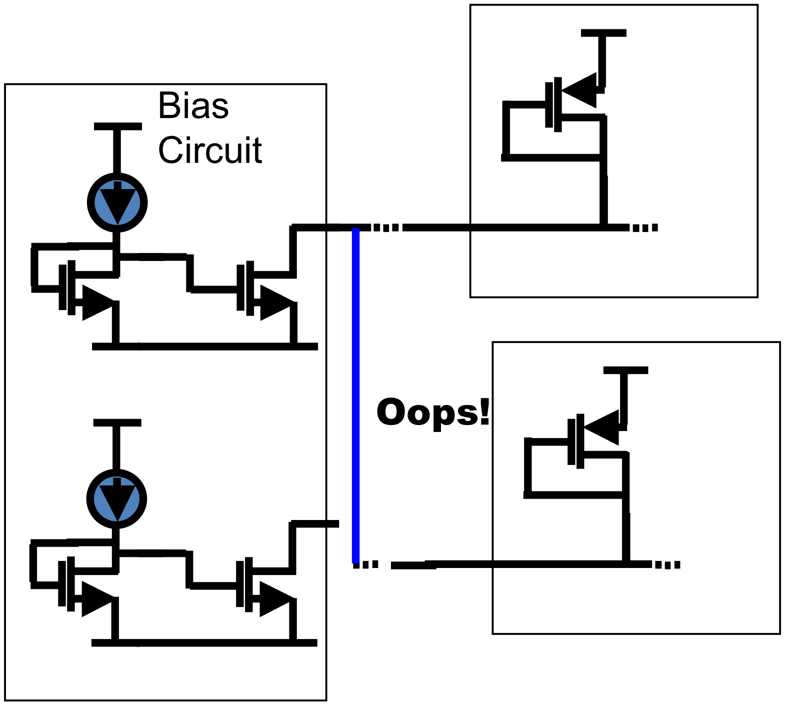
- 5.1 Bias current polarity error



- Designer of destination circuit intended to take current from a PFET source

5. Bias Current Errors

- 5.2 Bias current multiple sink error

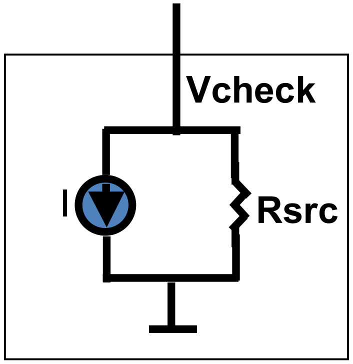


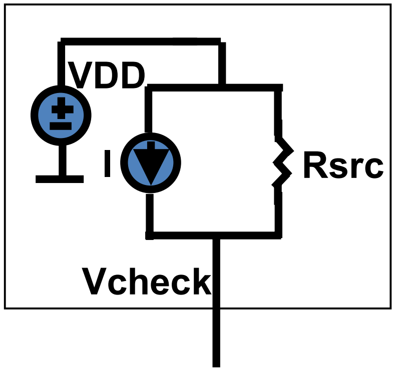
- Designers of different destination circuits took current from the same PFET source

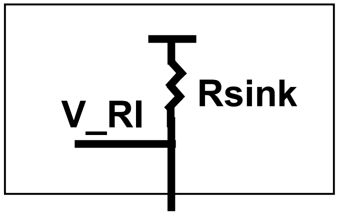
- **But of course, your team is too smart to make this kind of mistake, right?**

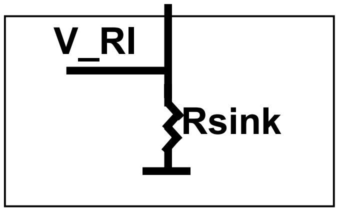
Catching Bias Current Errors

- Diagram of current source models:
  - Choose large Rsrc: I * Rsrc < VDD
  - If open circuited, Vcheck triggers an INFO message
- Diagram of destination current sink models (within larger block model):
  - **Choose a small Rsink, say 100 Ohms**
  - **Monitor V_RI**
  - **Incorrect polarity or incorrect current value becomes evident**







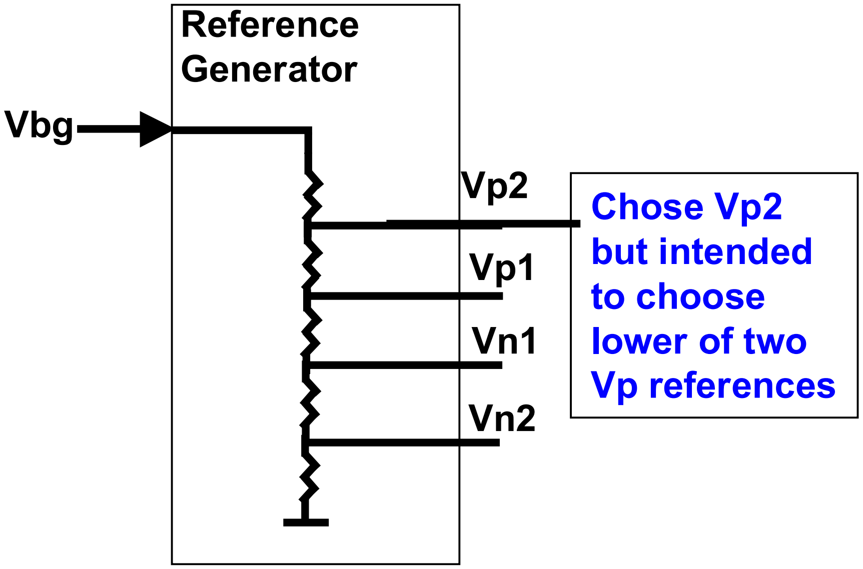


- Analog section of model continuously assigns V_RI = I * Rsink

- Digital section of model uses always @(above…) statements to trigger “good/bad” events as V_RI crosses thresholds
  - **“good” event allows normal operation**
  - **“bad” event displays error message and shuts down output.**

6. Reference Voltage Errors

- 6.1 Reference Voltage Choice Error

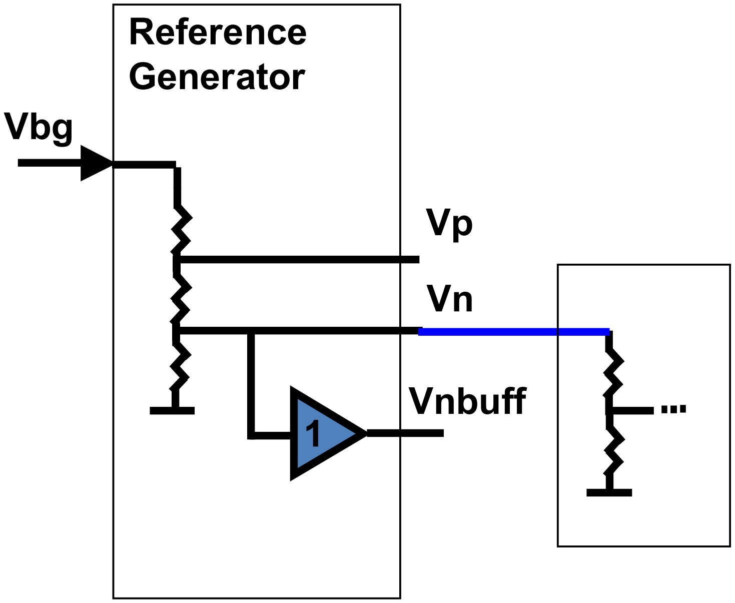


Chose Vp2 but intended to choose lower of two Vp references

- Sloppy naming convention led to designer choosing the wrong reference voltage

6. Reference Voltage Errors

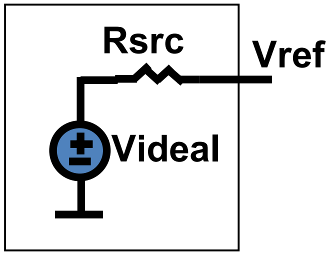
- 6.2 Reference Voltage Loading Error



- Oops! Drawing current from un-buffered reference voltage. Should have connected to Vnbuff

Catching Reference Voltage Errors

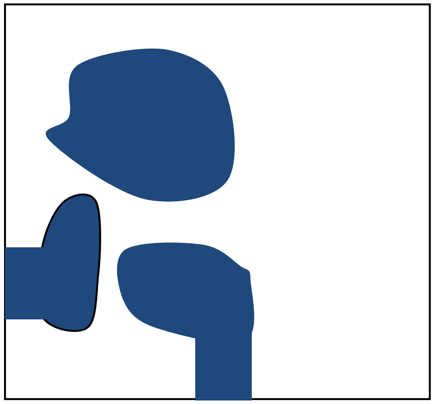
- Diagram of voltage source model:
  - Use realistic Rsrc found through circuit simulation or analysis



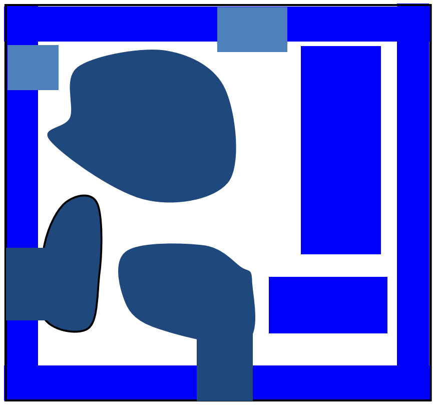
- Analog section models load resistance and voltage-division develops Vref to be monitored in the digital section
- Digital section of model uses always @(above…) statements to trigger "good/bad" events as Vref crosses thresholds
  - "good" event allows normal operation
  - "bad" event displays error message and shuts down output

Conclusion

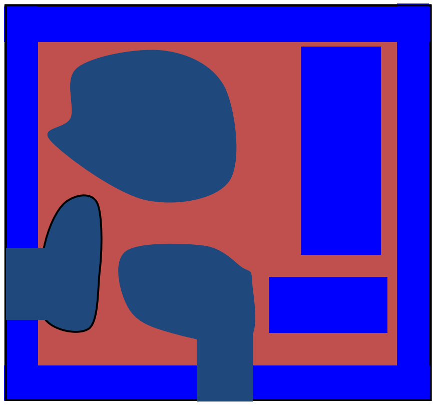
- There is no replacement for due diligence, concentration and thinking
- Top level simulations with behavioral models can increase your chances of getting all the bugs out of complex self calibrating systems
- Top level simulations with behavioral models are a powerful tool in your kit to fill the coverage gaps as below



Circuit Simulation of Analog Sections



Plus Digital Simulation of Digital Sections



Plus Top Level Simulation with Behavioral Models