Delta-Sigma Analog to Digital Converters – Report of Independent Study

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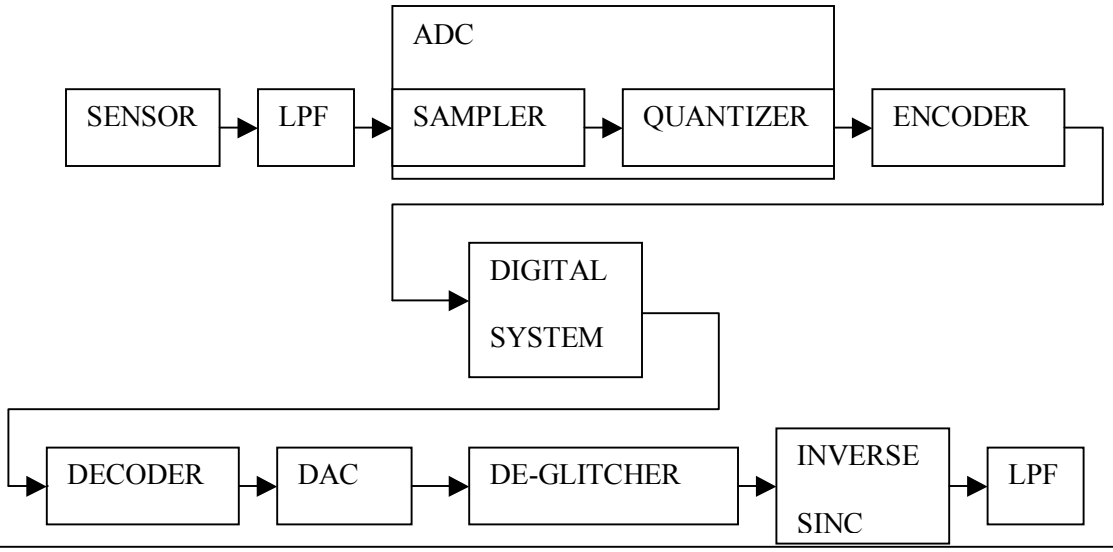
Abstract

This independent study was undertaken in order to learn to analyze, simulate, design and modify Delta Sigma Converters. The approach was to first gain a theoretical understanding of Delta Sigma Modulators (DSMs) by reading textbooks and journal articles. The second step was to become familiar with DSM operation and performance by simulating simple block diagrams out of textbook chapters. An excellent simulation tool for this is SIMULINK by MATLAB. The third step was to learn to use design tools for synthesizing and designing higher order DSMs. A free collection of MATLAB files was used to study a fourth order DSM. Finally, to gain familiarity with the low-level building blocks a second order DSM from a voice band CODEC was analyzed and simulated from the bottom up. This report, a study notebook, and a floppy disk containing the models and test programs I generated are submitted for grading.

Introduction

Human perceptions are analog, as are all naturally occurring signals. Data converters are the link between the real, analog world to the domain of digital signals. Communications, instrumentation, industrial controls, consumer electronics and medical imaging are some examples of systems using data converters.

Figure 1: GENERALIZED SYSTEM USING DATA CONVERTERS



Delta sigma modulators make up an important class of ADC that has been widely used in systems requiring high resolution at low or medium frequencies. High oversampling ratios and shaping of quantization noise are the distinguishing features of delta sigma converters. The essential principle is that feedback improves the effective resolution of coarse quantization.

Their popularity is due in part to the following characteristics:

- Reduced sensitivity to non-idealities of analog circuitry (such as op-amp gain and device mismatching) at the expense of digital complexity. As device sizes shrink so does the allowable maximum power supply voltage. Consequently, digital circuit density increases while analog circuit performance decreases, making the trade off between digital complexity and reduced sensitivity worthwhile.

- High oversampling rate simplifies the anti-aliasing filter requirements.

- Input sample-and-hold is not required if switched capacitor techniques are used.

This report is divided into the following sections:

1. Procedure: Describes why and how I went about this individual study.

2. Background: A summary of the theory behind delta sigma modulators.

3. Top-Down Analyses: Block diagrams of several delta sigma architectures are simulated.

4. Bottom-up Analysis: A delta sigma ADC is analyzed and simulated.

5. Summary

6. Appendices

7. References

1. Procedure

My objective in this individual study was to learn to analyze and design delta sigma converters. To do so, I read and studied from several textbooks [1-3] and compiled a notebook that I can continue to use as a ready reference. After gaining an understanding of the theory behind delta sigma modulators I built up and simulated some behavioral models in MATLAB. Finally I analyzed and modeled a delta sigma ADC that is part of the voice band circuit of a mixed signal cell phone integrated circuit with the intention making revisions.

This report, the behavioral models and my notebook are delivered as the outcome of my individual study.

2. Background

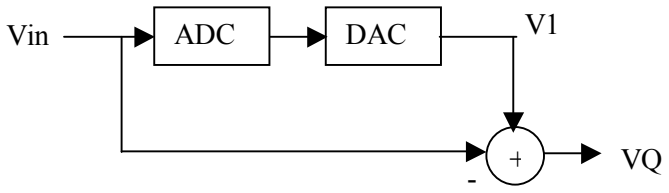
2.1 History

In 1952, the Delta Modulator was proposed by de Jager [4], which used a coarse quantizer and had a loop filter and DAC in the feedback path. The Error Feedback Coder was patented in 1954 by Cutler [5]. The problem with both of these was the requirement for high quality analog subtractors. Inose, Yasuda and Murakami [6] in 1962 took the Delta Modulator concept and moved the loop filter (integrator) into the forward path before the quantizer and renamed it Delta Sigma – for Delta Modulator and Sigma for the summation

done by the integrator. It seems that "Sigma Delta" rolls off the tongue more easily than "Delta Sigma" and that term somehow came into use. Both are used interchangeably.

2.2 Delta Sigma Basics

2.2.1 Quantization Noise



Quantization noise analysis is developed in the Johns textbook [3] and is summarized here. In the above block diagram, $VQ = V1 - Vin$ and obviously $V1 = Vin + VQ$. That is, the DAC output exactly equals the input plus quantization noise, which is a deterministic function of the input. When Vin is a ramp, V1 is a staircase and VQ is a sawtooth pattern with zero mean and amplitude one-half the LSB size. (Assume without loss of generality that the ADC and DAC have the same LSB size.) The RMS value of VQ can be determined as follows:

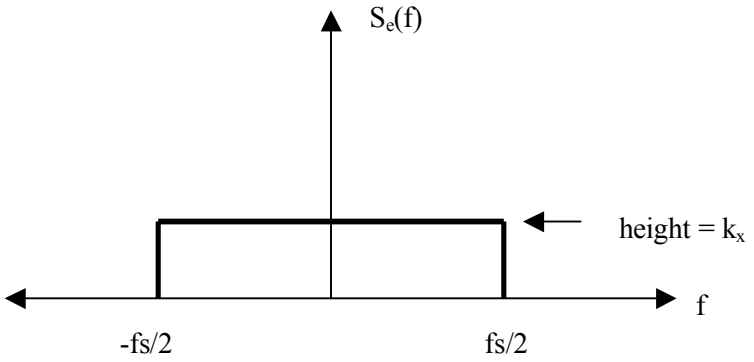
$$VQ_{RMS} = \left[\frac{1}{T} \int_{-T/2}^{T/2} VQ^2 dt \right]^{\frac{1}{2}} = \left[\frac{1}{T} \int_{-T/2}^{T/2} V^2{}_{LSB} \left(\frac{-t}{T} \right)^2 dt \right]^{\frac{1}{2}} = \frac{V_{LSB}}{\sqrt{12}} = \frac{\Delta}{\sqrt{12}}$$

Each additional bit of resolution divides Δ by 2, so that noise power is reduced by 6 dB for each additional bit.

The ideal signal to noise ratio is then $SNR = 20\log\left(\frac{Vin_{RMS}}{VQ_{RMS}}\right)$.

For a sinusoidal Vin with amplitude Vref/2 this becomes

$SNR = 20\log\left(\frac{Vref/2\sqrt{2}}{\Delta/\sqrt{12}}\right) = 6.02N + 1.76dB$. Noise power, P_e is the square of the RMS value of VQ, or $\Delta^2/12$ independent of the sampling frequency, fs. Assuming a flat power spectral density, $S_e(f)$, for VQ within +/- fs/2:



The quantization noise power is the (area under $S_e(f))^2$. That is,

$\int_{-fs/2}^{fs/2} k_x{}^2 df = k_x{}^2 \cdot fs$ and this equals $\Delta^2/12$, so the height of $S_e(f)$, $k_x = \frac{\Delta}{\sqrt{12\,fs}}$.

VQ is a deterministic function of Vin, but with an actively varying Vin(t), VQ becomes nearly random with noise power P_e.

2.2.2 Oversampling and Noise Power

If Vin(t) has bandwidth f_0 and is sampled at fs, then the oversampling ratio is defined as, OSR = fs/(2f_0). Since there are no frequencies of interest between f_0 and fs, we can apply an ideal filter H(s) with cutoff at f_0 to get noise power

$$P_e = \int_{-fs/2}^{fs/2} S_e^{\,2}(f)\,|H(f)|^2\,df = \int_{-f_0}^{f_0} k_x^{\,2}\,df = 2k_x^{\,2} f_0 = 2f_0 \frac{\Delta^2}{12\,fs} = \frac{\Delta^2}{12}\frac{1}{OSR}$$

From this it can be seen that doubling the OSR reduces the noise power by one-half so there is 3 dB per octave noise power reduction.

2.2.3 Noise Shaping

Here's a simplified block diagram of a delta sigma modulator

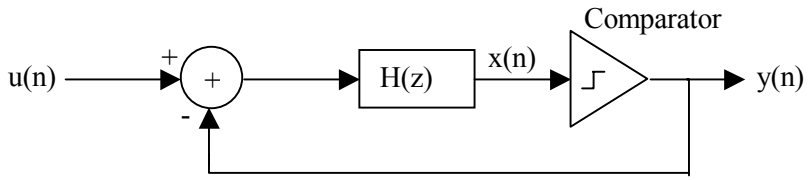


Figure 2: Delta Sigma Modulator

The comparator or one-bit quantizer makes the system non-linear and difficult to analyze. We can linearize the system by making use of the fact that the quantizer output is equal to its input plus quantization noise. By arguing that the quantization noise is nearly random for an active input signal u(n), we replace the comparator with a summation of x(n) and e(n) as follows:

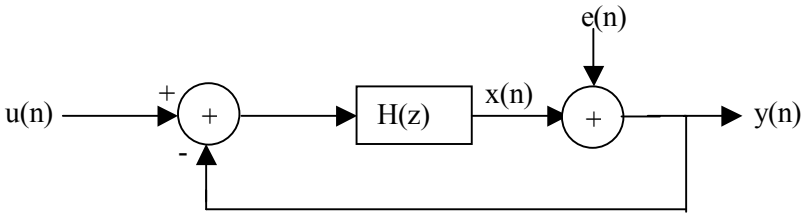


Figure 3: Linearized Delta Sigma Modulator

In this diagram, we superpose outputs due to u(n) and e(n) to get y(n). Transfer functions are defined from each input to the output. We have the signal transfer function

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)}$$

And the noise transfer function

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}.$$

The remaining task is to choose H(z) to have a large magnitude from 0 to f_0 so that $STF(z) \cong 1$ and $NTF(z) \cong 0$ over the bandwidth of interest. A simple first order transfer function that meets this requirement is $H(z) = \frac{1}{z-1}$, which can be realized as follows:

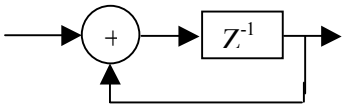


Figure 4: First order H(z)

Substituting this H(z), we get the expression

$$Y(z) = STF(z)U(z) + NTF(z)E(z) = z^{-1}U(z) + (1 - z^{-1})E(z)$$

STF(z) is simply a delay. NTF(z) performs time domain differentiation – high pass filtering. Each sample is subtracted from the previous one. At DC, each sample is identical so subtraction results in zero. At low frequencies, the signal can't change very much from sample to sample so the difference is rather small. At higher frequencies large differences are more likely, thus H(z) serves to reduce the noise within the band of interest, letting it increase outside of that band. This is what's known as noise shaping. The combined advantages of noise shaping and noise reduction through large oversampling ratios are what make delta sigma modulation practical.

Higher performance is realized with higher OSR, multiple bit quantization and higher orders H(z),. The difficulties of higher OSR are the usual challenges of high frequency circuit design. Increasing the number of quantization levels introduces errors due to gain, offset and non-linearity – similar problems to those of Nyquist rate converter design. Use of multi-bit quantization also requires multi-bit D/A conversion in the feedback path. It turns out that the overall linearity of the converter is no better than the linearity of the feedback D/A. Increasing the order of H(z) is the usual approach to higher performance, along with maximizing OSR. Many H(z) architectures have been invented, each with its advantages and difficulties. The standard H(z) for voice band telephony is a second order with a single feedback loop, which will be analyzed and simulated later. The standard architecture for high quality audio is a fourth order H(s).

2.2.3 DC Example

Here's a hand worked example of first order delta sigma conversion of a DC signal. In the following diagram, the output of the quantizer is +/- 1 so there is no need for an explicit DAC. The input u(n) is 1/3 and assume x(0) is 0.1.

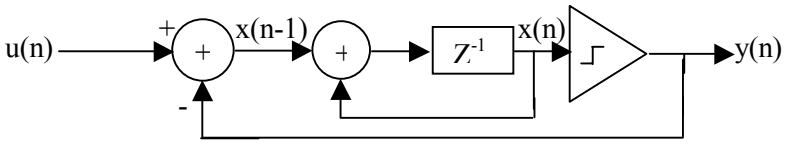


Figure 5: First Order Delta Sigma Modulator

Table 1: Node Value Sequence for U(n) = 1/3 and X(0) = 0.1.

N	X(N-1)=U(N)-Y(N)+X(N)	X(N)	Y(N)	E(N)=Y(N)-X(N)
0	-0.567	0.1	1	0.9
1	0.767	-0.567	-1	-0.433
2	0.1	0.767	1	0.233
3	-0.567	0.1	1	0.9
4	0.767	-0.567	-1	-0.433
5	0.1	0.767	1	0.233
6	-0.567	0.1	1	0.9

Observations:

- The average value of y(n) is 1/3, which exactly equals the input.
- The noise signal e(n) is not nearly random. This is expected since u(n) is not "active".
- The noise signal is periodic with period $T_e = 3 \cdot T_s$ and will produce a tone at 1/3 fs.

2.2.4 Encoding the Output

That the average value of y(n) is the digital representation of the analog input is an important point. Following y(n) are digital signal processing stages that further reduce quantization noise and by filtering and down-sampling (decimation) find a running average of y(n) so that the ultimate output is a sequence of words N-bits wide.

Here is a block diagram of a typical digital signal processing section for a delta sigma modulator:

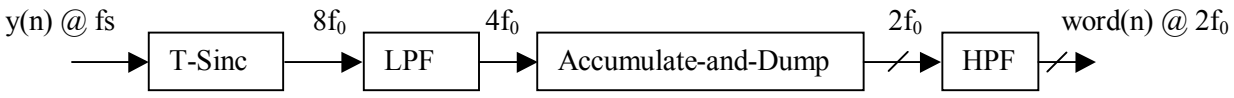


Figure 6: DSP Section for Delta Sigma Modulator

The T-Sinc stage down-samples the y(n) bit-stream and removes some of the quantization noise. Its order is one higher than L, the order of the modulator's loop filter. It consists of L+1 integrators connected to L+1 differentiators by a switch operating at frequency $8f_0$. Its name comes from the form of its transfer function which is Sinc(Mx)/Sinc(x). A typical

LPF is fourth order with a seventh order numerator. The extra zeroes compensate for the sin(x)/x roll-off of the T-sinc stage. The accumulate-and-dump and high pass stages complete the task of forming the Nyquist rate output words.

Delta sigma modulator architectures are now very well known and there are software packages available (some even free) to help with selection and simulation of both the modulator and DSP sections. One example [7] was downloaded from the MATLAB web site and used for this report.

3. Top-Down Analyses

Several block diagrams of delta sigma modulators were simulated with MATLAB and SIMULINK. First and second order systems were created in simulink and a fourth order system was synthesized and simulated using [7].

3.1 First Order

The first order delta sigma modulator of Figure 5 was modeled in MATLAB/SIMULINK.

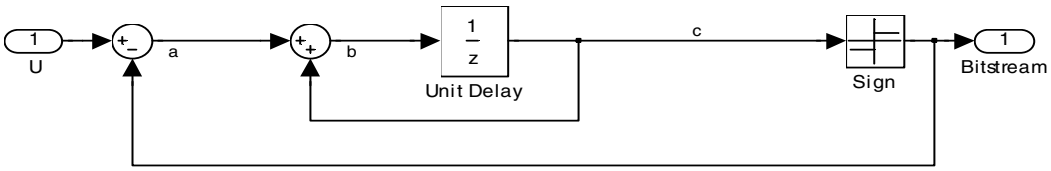


Figure 7: Simulink Model of First Order DSM.

Its corresponding DSP is below:

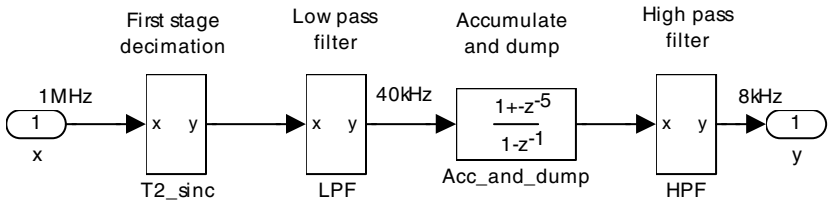


Figure 8: DSP for First Order DSM

The DSM and DSP were inserted into the test page below:

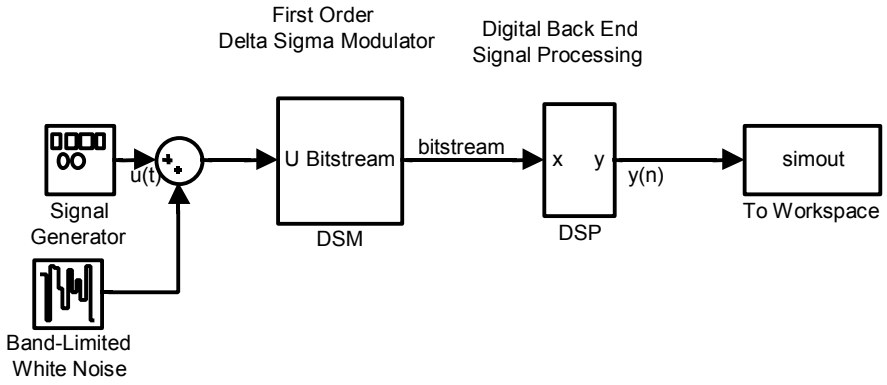


Figure 9: Test Page for First Order DSM

This was tested with a 1 kHz sine wave with amplitude 0.8V, with and without $50uV_{RMS}$ noise. (Recall that the DAC feedback was +/- 1.0V). The model returns the time domain output to the MATLAB workspace, where it is truncated to 16 bit words before Fourier analysis. The magnitude plot of the spectrum follows. Observe that the system produces harmonics at 2 and 3 kHz at about 67 dB down from the fundamental. These are idle tones similar to the ones observed in the DC experiment of Table 1. The blue simulation shows that $50uV_{RMS}$ additive noise at the input does not degrade the performance.

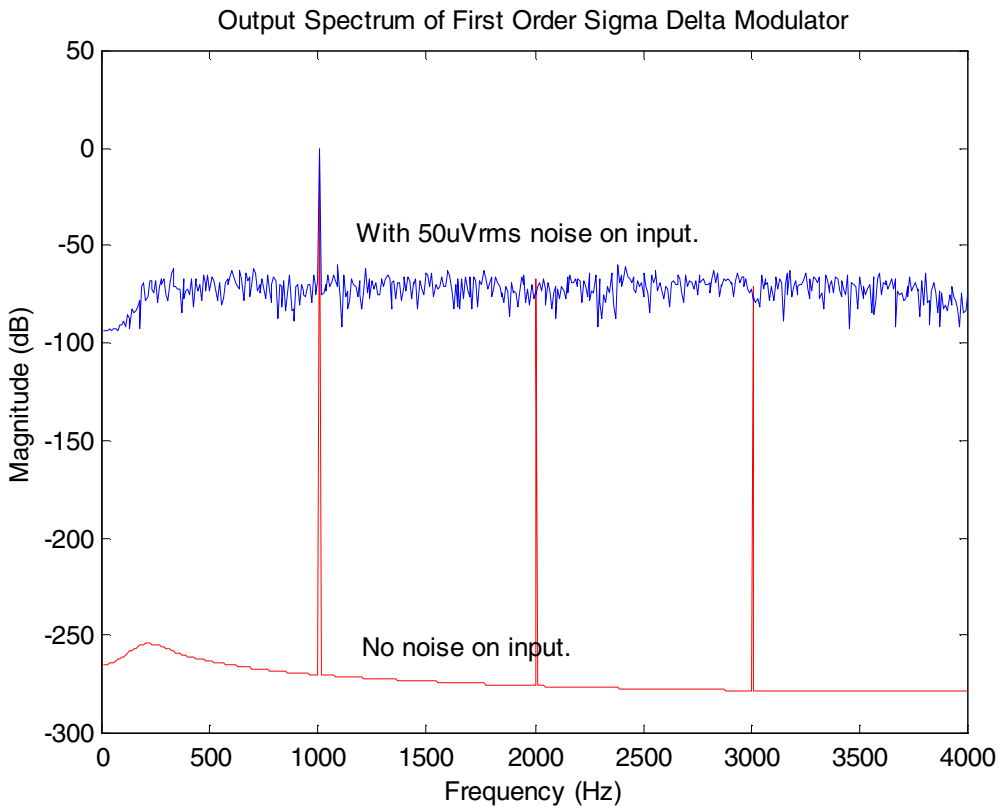
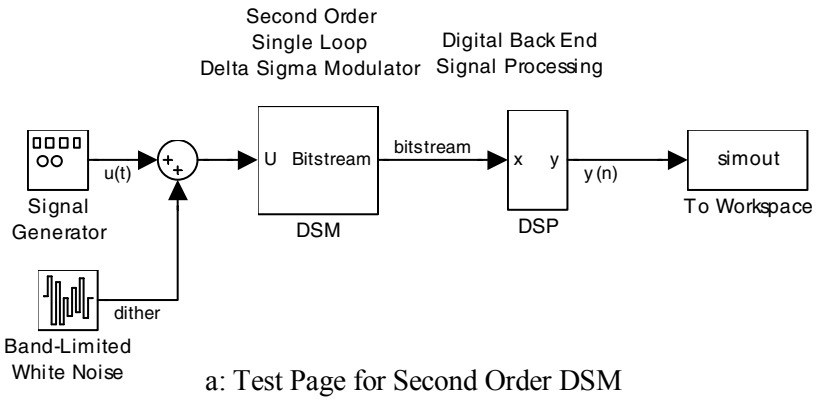


Figure 10: MATLAB First Order DSM Simulation Results

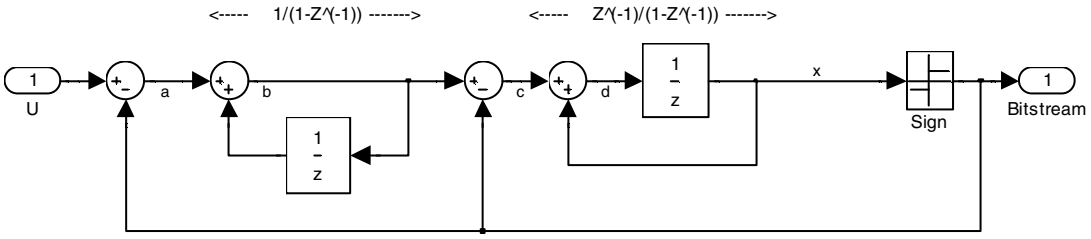
In fact, human hearing is sensitive enough to detect the idle tones even when embedded in noise. Were this system to be implemented, a dithering scheme would be used to break up the idle tones. Dithering can be accomplished by pseudo-randomly varying the comparator's trip point between two slightly different levels.

3.2 Second Order

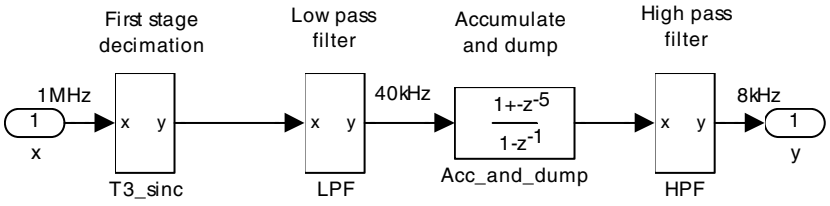
A second order DSM implementing the function $Y(z) = z^{-1}U(z) + (1 - z^{-1})^2 E(z)$ was modeled in MATLAB/SIMULINK. Figure 16 shows its modulator, DSP and test page models. The two stages of the loop filter implement $\frac{1}{1-z^{-1}}$ and $\frac{z^{-1}}{1-z^{-1}}$.



a: Test Page for Second Order DSM



b. Second Order DSM



c. DSP for Second Order DSM

Figure 11: Second Order DSM Model

The second order model was tested with a 1 kHz signal, with and without $10uV_{RMS}$ noise. The magnitude plot of the spectrum follows. There is no 2 kHz harmonic with this system. The 3 kHz harmonic is about 79 dB down. The upper (blue) trace shows that $10uV_{RMS}$ noise at the input brings the noise floor up to the level of the third harmonic.

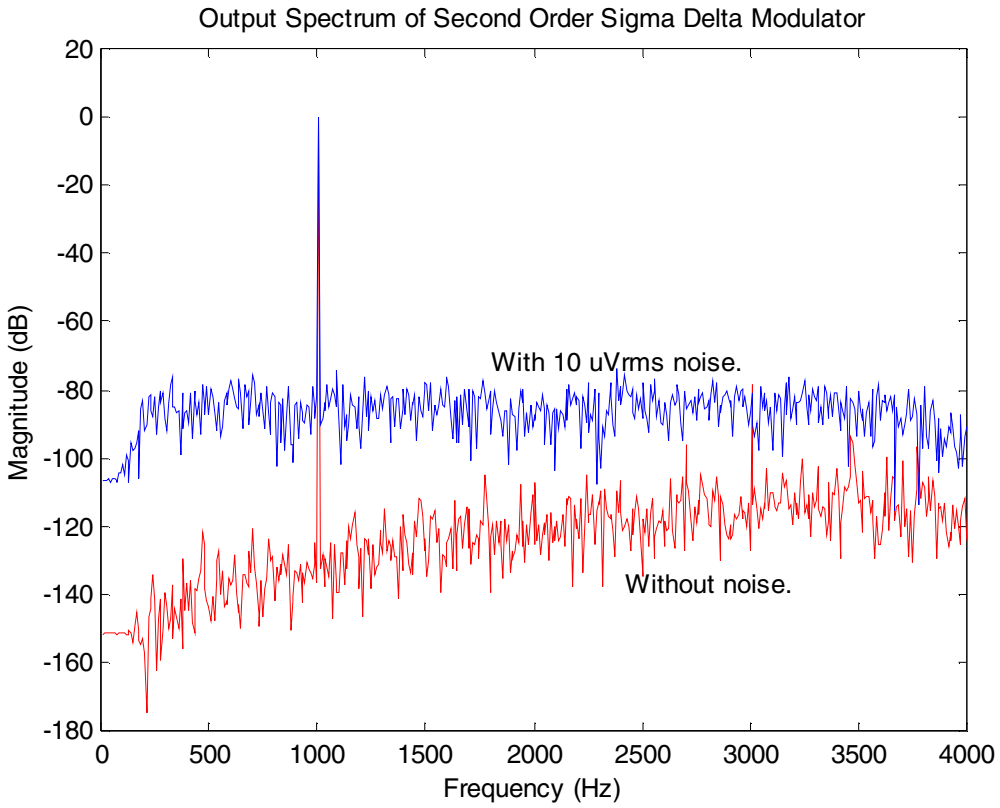


Figure 12: Second Order DSM Simulation Results

The next figure shows the superimposed results of tests at frequencies ranging from less than 100 Hz to over 3.5 kHz. The filter is flat in band and rolls off at the low and high ends.

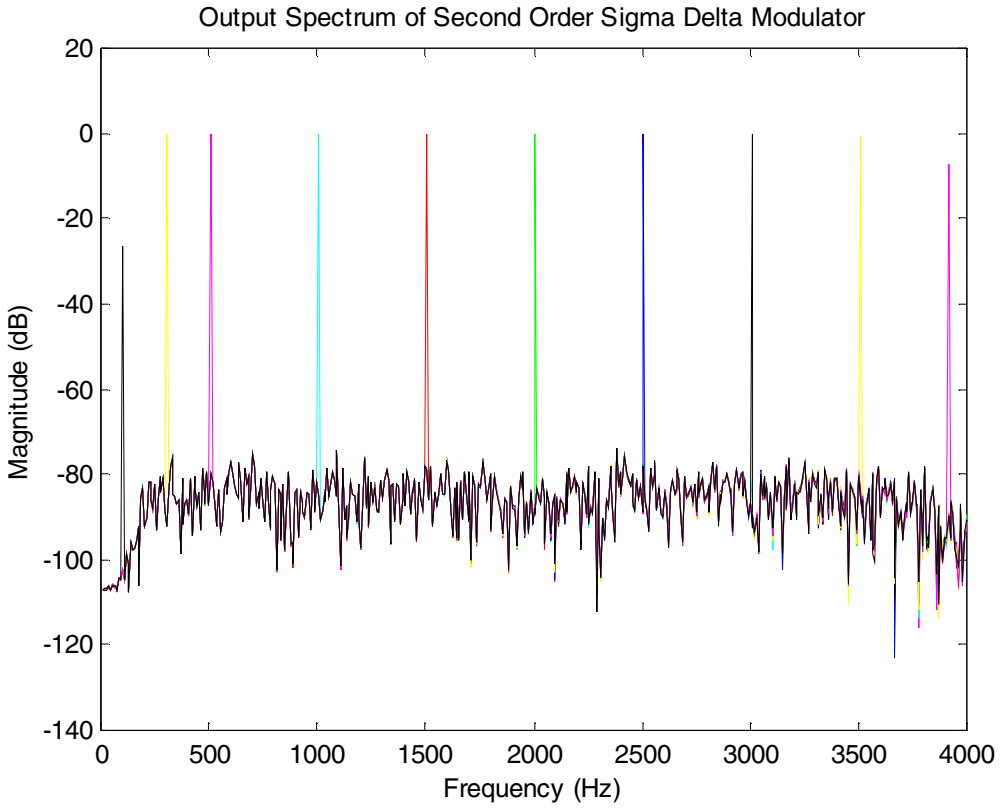


Figure 13: Second Order DSM Results at Different Frequencies

3.3 Fourth Order

The Delta-Sigma Toolbox [7] from MATLAB was used to design and simulate a fourth order converter. This toolbox is available free of charge on the MATLAB website. The Cascade of Integrators, Feed Back (CIFB) structure was chosen for this exercise. The block diagram is shown below in Figure 14.

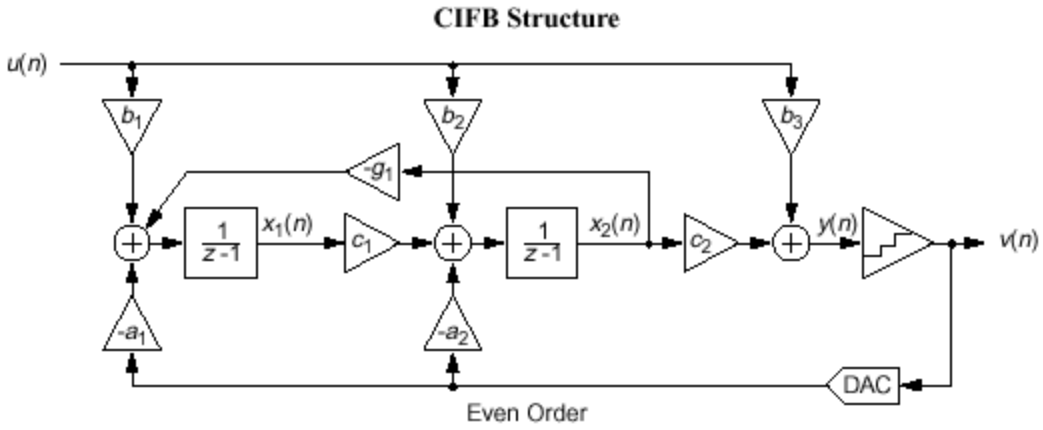


Figure 14: Block Diagram of CIFB Structure Used for Fourth Order DSM Exercise.

The steps to populate the variables in the above structure are:

1. H=synthesizeNTF(4,250,1): Synthesize a fourth order NTF with OSR of 250 (1MHz/4kHz). The third argument of 1 sets a flag to optimize the zero placement of the NTF.

2. [a,g,b,c]=realizeNTF(H,'CIFB'): From the NTF synthesized in step 1 populate the a, g, b and c vectors which are the (unscaled) gain coefficients of the CIFB DSM of Figure 14.

3. ABCD = stuffABCD(a,g,b,c,'CIFB'): Reformat the vectors into the ABCD structure needed for the next step.

4. [ABCDs,umax]=scaleABCD(ABCD,2,0,1): Iteratively simulate and scale the ABCD matrix to optimize the dynamic range of the internal states. The second through fourth arguments specify: 2-level quantizer, optimized at frequency = 0, limit the state

variable magnitude to 1.0. The returned value umax is the maximum input amplitude for stable operation.

5. [an,gn,bn,cn]=mapABCD(ABCDs,'CIFB'): Reformat the scaled matrix into the vector form.

6. [ntf,stf]=calculateTF(ABCDs,1): Calculate the NTF and STF for the scaled system. Compare this to the NTF synthesized back in step 1.

7. v = simulateDSM(u,ntf): Perform a time domain simulation and Fourier analysis of the scaled system.

For the scaled fourth order DSM, the resulting coefficients are:

umax = 0.6067

a = [0.4009 0.3762 0.4105 0.5865]

g = [0.2050 0.2141] * 10^{-3}

b = [0.4009 0.3762 0.4105 0.5865 1.000]

c = [0.0890 0.2289 0.5470 1.3736]

The NTF is $\frac{(z^2-2z+1)(z^2-2z+1)}{(z^2-1.493z+0.6647)(z^2-2z+1)}$.

Figure 15 compares simulated versus predicted SNR across a range of input amplitudes. Peak SNR is 161.1 dB.

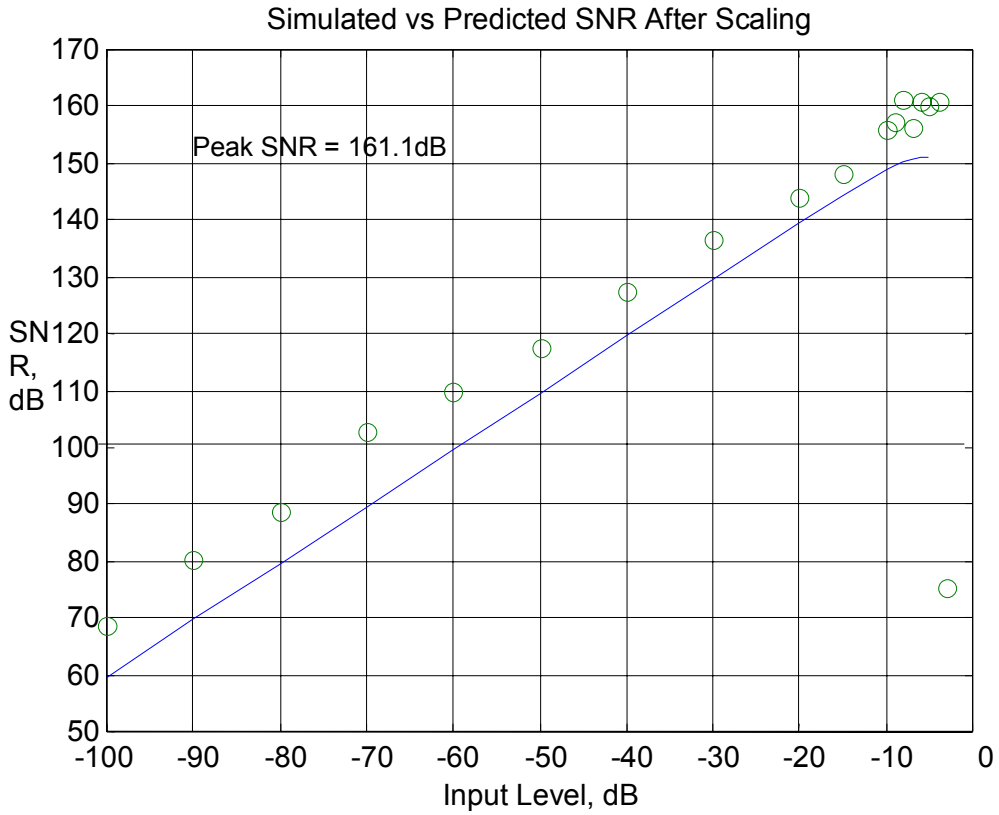


Figure 15. Simulated vs Predicted SNR for 4th Order DSM

Figure 16 is the noise transfer function magnitude response. The top graph shows the band up to the sampling frequency, and the bottom graph shows only the signal bandwidth. Within the signal band, the rms quantization noise gain is –130 dB.

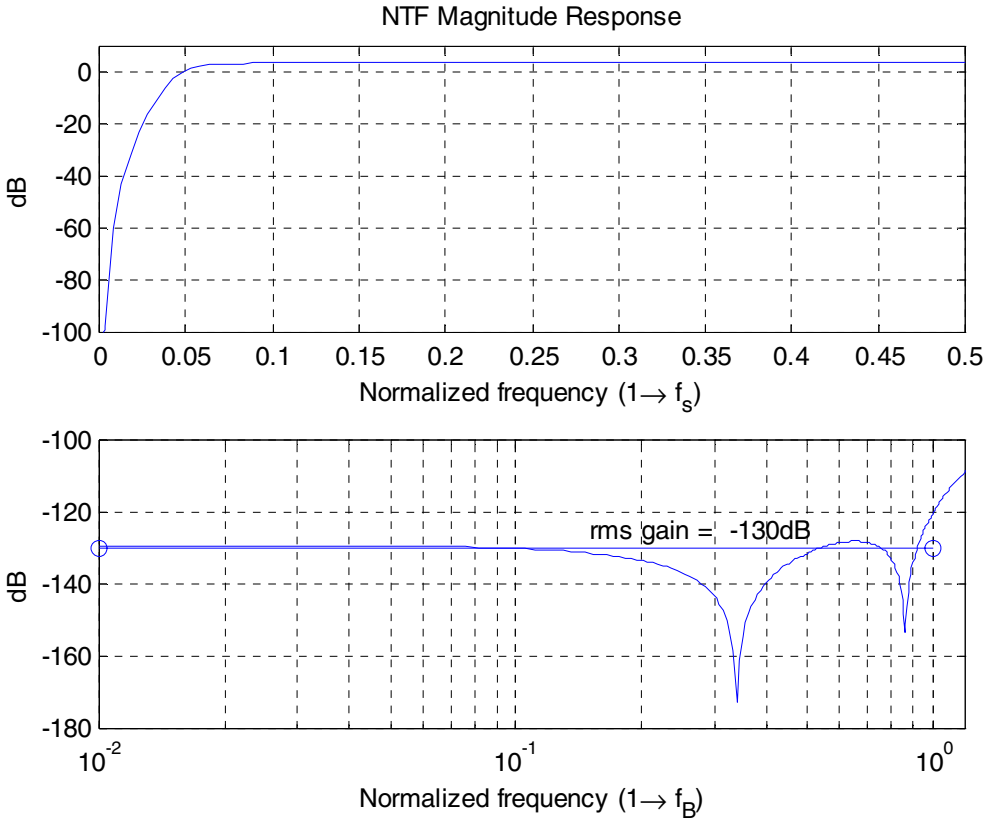


Figure 16: NTF Magnitude Response

Figure 17 shows the time domain input waveform and output bit stream. At this oversampling rate, you can see the density of transitions is proportional to the slope of the input.

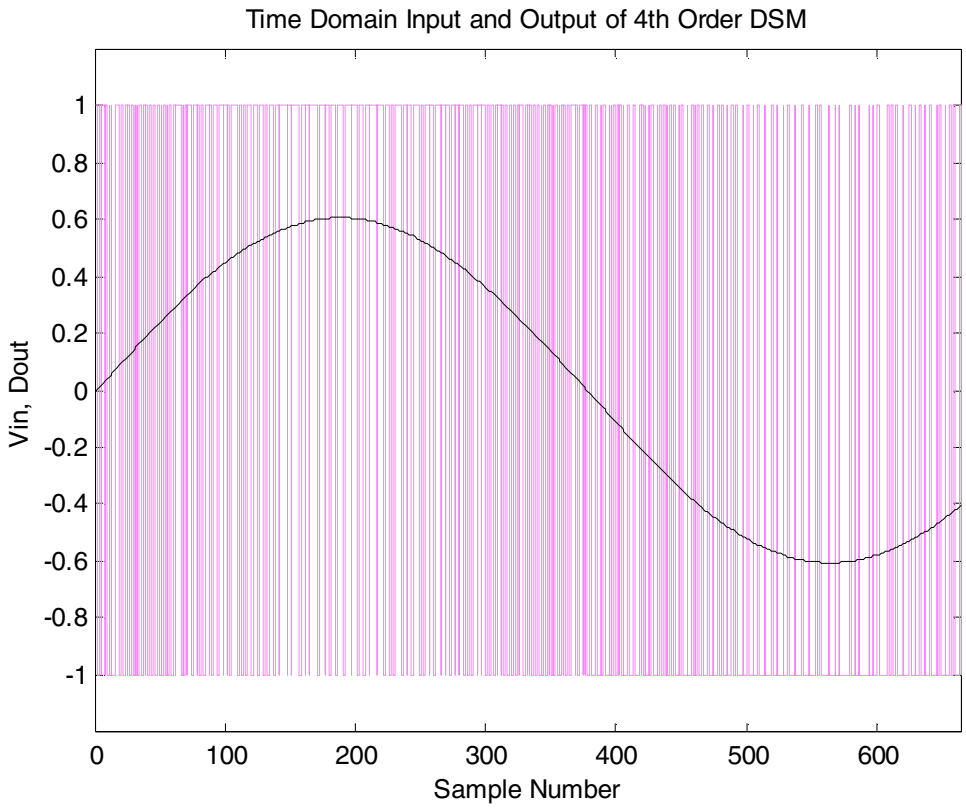


Figure 17: Time Domain Input and Output Plot

Figure 18 shows the spectrum of the test output, up to the sampling frequency. Noise shaping is obvious.

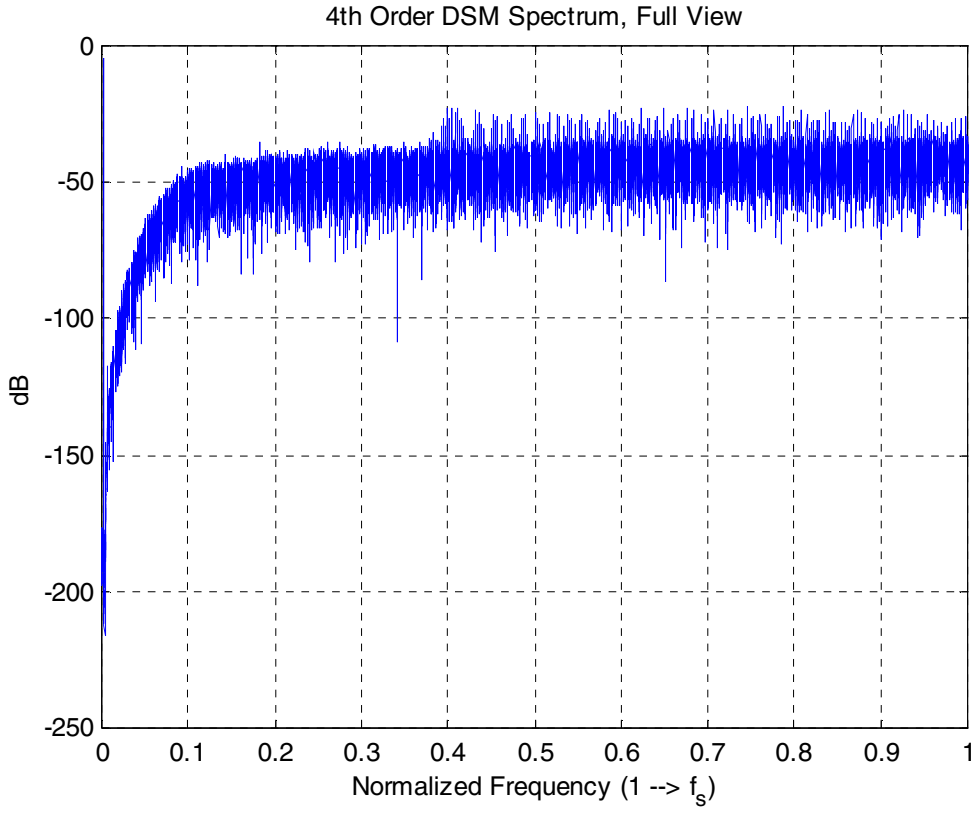


Figure 18: Spectrum of transient simulation output

Figure 19 is a close-up of the Nyquist band. SNR is 158 dB within the band of interest.

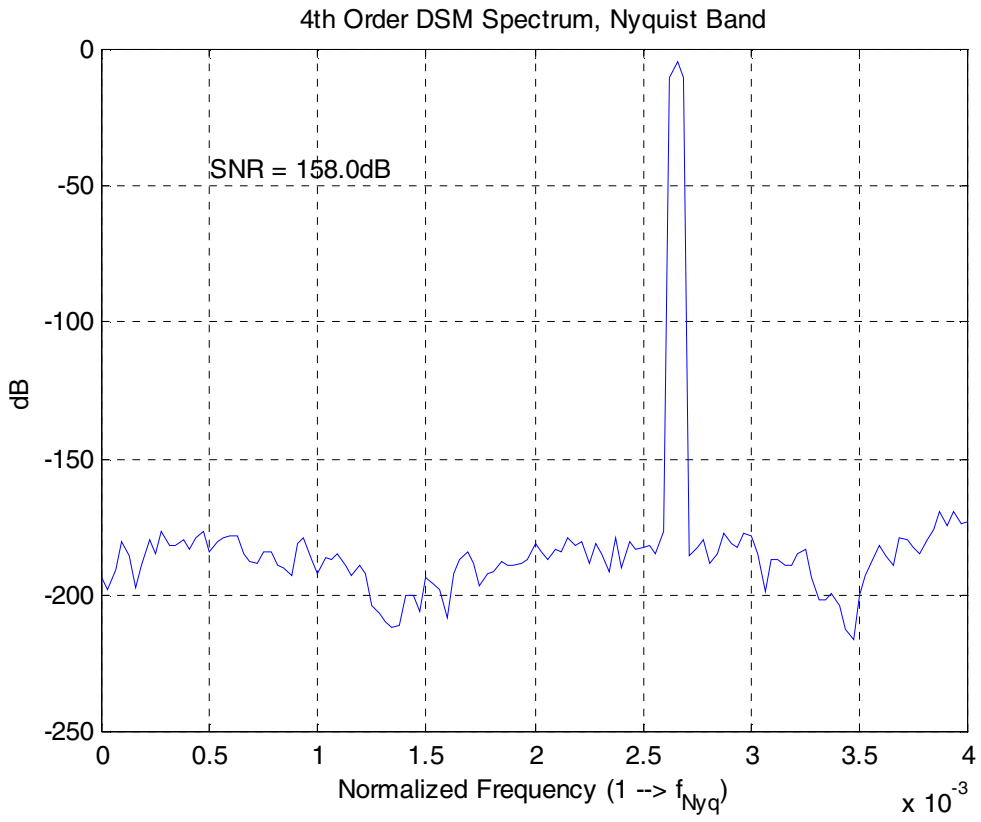


Figure 19: Spectrum of Transient Simulation, Nyquist Band

4. Bottom-Up Analysis

For this part of the study, the schematics for a second order DSM were analyzed to develop Z-domain transfer functions. From there, a MATLAB/SIMULINK block diagram was created and simulated. The schematic page is similar to that of a DSM used in a voice band CODEC -- part of a Conversion Signal Processor IC from a cell phone handset. They have been redrawn by hand to avoid any appearance of compromising proprietary information.

4.1 Circuit Description

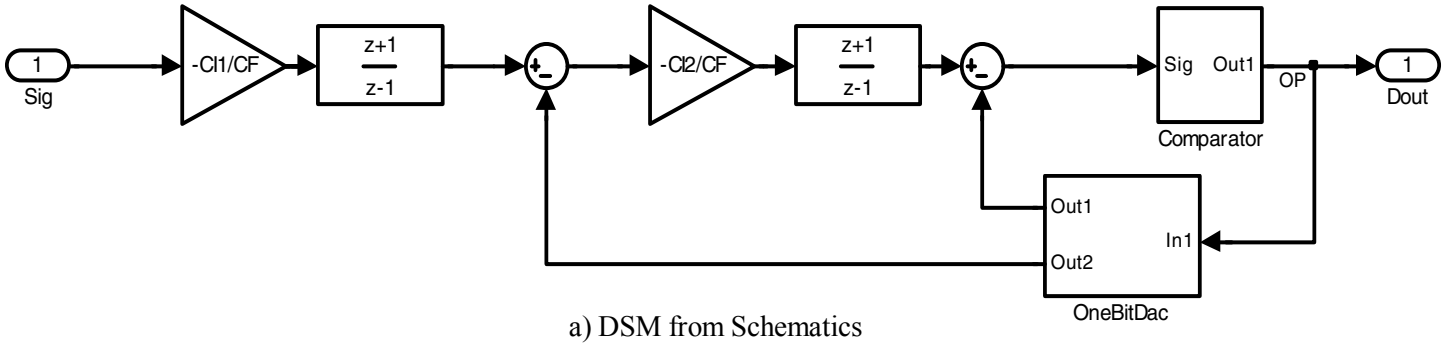
The simplified schematic is page A1 in the appendix. The first differential op-amp along with its feedback capacitors CF , the input switched capacitors CI1 and the DAC input switched capacitors CX form the first integrator stage. The second integrator stage has the same values of CF and CX but different values for CI2 . The second integrator stage goes to a differential latched comparator that generates the outputs OP and ON. A table defines the comparator operation. OP, ON and the two clock phases go to a logic block (described in a table) that controls the DAC feedback switches with signals X1 and X2.

4.2 Circuit Analysis

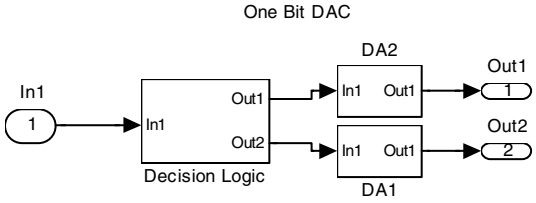
Appendix pages A2 – A5 show the conservation-of-charge analysis used to develop the transfer function. On those pages, equations 4-6, 10-11 define the transfer functions for all output combinations.

4.3 Simulink Model

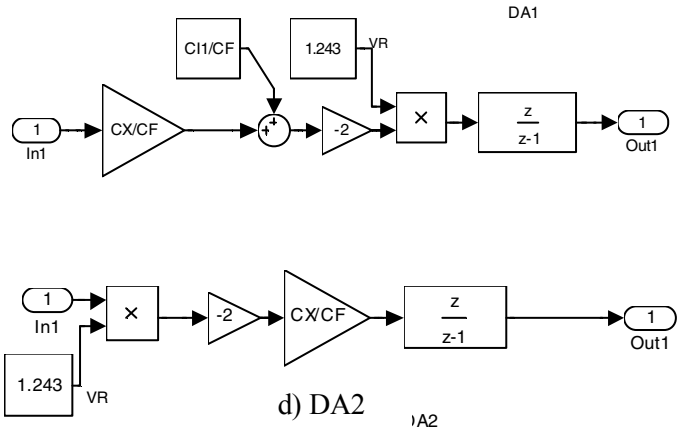
The five transfer functions were then combined with logic controls and implemented in a Simulink model. Key views of that model appear in Figures 20 and 21.



a) DSM from Schematics



b) One-Bit DAC



d) DA2

Figure 20 : SIMULINK Model of DSM

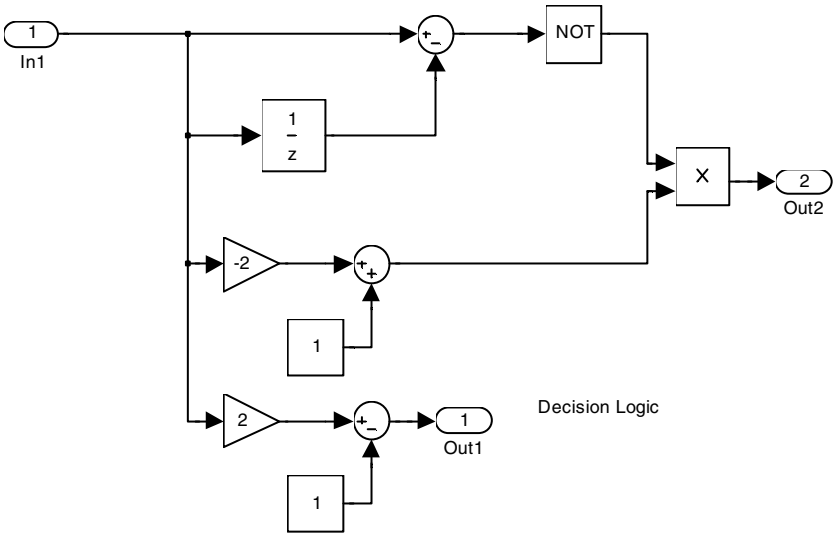


Figure 21: Decision Logic for One-Bit DAC

4.4 Simulation Results

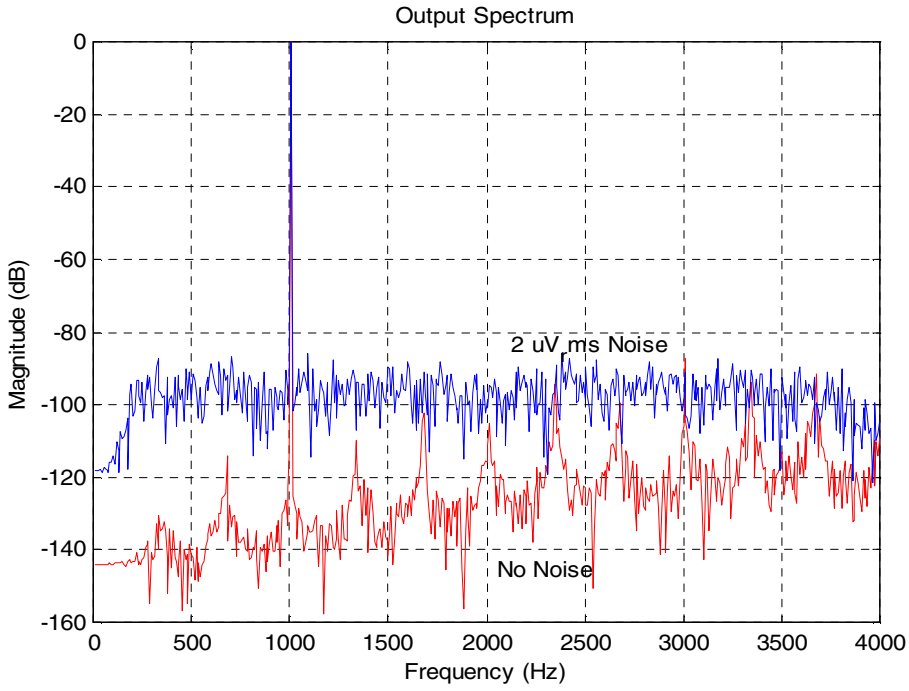


Figure 22: Output Spectra, With and Without Noise

The DSM model was inserted into the test circuit shown previously in Figure 11.a. The results shown above in Figure 22 show it achieves about 88dB SNR with and without $2uV_{RMS}$ noise added to the input.

5. Summary

By reading, studying, analyzing, designing and simulating delta sigma modulator ADCs I have reached my objective – to prepare myself for designing DSMs into voice band signal processor integrated circuits. The theoretical background came from several textbooks. No one of them in my opinion is a good tutorial by itself. Going directly from theory to block diagram simulations of first and second order DSMs provided insight into their operation and performance. Using the MATLAB toolbox to work with a fourth order system provided further insights. But the most satisfying part of this study was working backwards from the schematics to develop a model to simulate a real second order DSM. I'm prepared now to go on and further optimize this circuit for the next version of the IC.

Furthermore, this study has piqued my curiosity to the extent that I've chosen delta sigma modulators to be the topic of my dissertation. Immediately upon completion of this report, I plan to write the Proposal for Dissertation.

Appendices

Appendix pages A1 to A5 follow. A1 is the simplified schematic of a second order delta sigma ADC from industry. Pages A2-A5 are the hand analysis leading to transfer functions for that ADC.

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