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An Efficient Low-Power Audio Amplifier With Power Supply Rails Tracking The Output By Means Of Pulse Width Modulation

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ABSTRACT

A low-power audio amplifier with pulse width modulated power supply rails that track the output signal is presented. Because of the tracking power supply rails, the voltage drop over the power transistors is kept as low as possible and nearly constant, so that power efficiency remains high for low as well as high output level signals. A very simple digital input pulse width modulation scheme provides four power rails to a fully differential class-AB power amplifier. The simplicity of the circuit makes it an attractive solution for low cost portable audio applications, instead of using a more complex pulse width modulated class-D audio amplifier. An efficiency increase of about 10% has been simulated over the same class-AB output stage using fixed DC rails of 3 Volts and 0 Volts, with very little sacrifice in THD. Also presented are results from a 12-Volt, single-ended hardware prototype of the system.

1. INTRODUCTION

The goal of extending battery life for portable consumer audio devices motivates the ongoing quest for higher efficiency power amplifiers. In a highly efficient system, the power dissipated in the amplifier electronics is much lower than that delivered to the speakers.

Class-AB is a traditional architecture for a highly efficient audio amplifier [1]. However, the apparent high efficiency of class-AB only exists at full-volume operation, which is hardly the usual case. At typical listening levels the efficiency is much lower. This phenomenon has brought about the concept of weighted-efficiency [2]. High weighted-efficiency means the system is efficient under the most usual operating conditions. For instance, if a system is operated at 40% of full volume 80% of the time, then it is more important that the system be efficient at 40% than at full volume.

Several different power amplifier structures are available for increasing the relatively low efficiency of class-AB amplifiers. Class-D amplifiers are one such scheme [3]. Class-D amplifiers make use of pulse width modulation (PWM), wherein power MOSFETs operate as switches and are either completely cut off and dissipating no power, or are completely on with ideally no resistance and again, dissipating no power [4]. PWM systems have been described in the literature ranging from mostly analog to mostly digital, and each has its problems and advantages [3-15]. The main disadvantages of class-D are distortion, and the complexity and size that are required to reduce distortion [12]. Section II-E discusses this in more detail.
To solve all these problems, this paper presents an audio amplifier system including a fully differential class-AB power amplifier whose four output power rails are made to track its differential outputs by means of class-D pulse-width-modulated digital-to-analog conversion. A working name for the system is PWM-PAMP for PWM-Powered Amplifier.

The remainder of this paper is divided into six sections. Section 2 defines efficiency and gives a brief overview and comparison of amplifier classes A, B, AB and D (Pulse-width modulation). Section 3 shows how the low weighted-efficiency of class-AB, and the distortion or size/complexity disadvantages of class-D can be overcome by PWM-PAMP and describes its architecture, circuitry and analysis. In section 4 the schematic and behavioral model implementation of PWM-PAMP is described. Section 5 presents the simulated results. Section 6 presents a hardware prototype using discrete components and oscilloscope plots of its operation. Finally, section 7 gives conclusions and discusses further work.

2. AMPLIFIER CLASSES A, B, AB AND D

A useful definition of efficiency is the ratio of the power used to the power supplied. In a 100% efficient audio system, all the energy would be converted to mechanical (sound) energy and no power would be dissipated in the amplifier itself. This would be true for low as well as high speaker volume.

2.1. Class-A Amplifiers

Fig. 1 shows an output stage of the power amplifier that can be used to compare the operation and efficiency of classes A, B and AB [16]. For class-A operation, Vbias [P, N] are chosen such that ID [1, 2] are always greater than Isat. The average current is ID, independent of signal amplitude.

Although this is amplifier architecture is highly linear it is not practical for battery-operated applications. Class-A efficiency is always less than 50% and goes to zero as the output voltage goes to zero. The expression for efficiency derived in [16] is

$$\eta = P_L / P_S = \tfrac{1}{2}\left[\frac{V_L}{V_{L\max}}\right]^2 \frac{1}{1+R_{DSon}/R_L}\frac{1}{1+2\gamma}$$

where $\gamma = I_{SAT} / I_{L\max}$ and $I_{L\max} = V_{L\max} / R_L$.

2.2. Class-B Amplifiers

Fig. 2 shows that same output stage biased as class-B. Only one device is on at a time. There is zero quiescent current (i.e., when Vi = 0). Efficiency improves at the expense of crossover distortion.

Class-B efficiency, which can be expressed [16], as $\eta = \frac{\pi}{4}\frac{V_L}{V_{L_{\max}}}\frac{1}{1+R_{DS_{on}}/R_L}$ has an upper bound of $\pi/4$ or 78.5%, and goes to zero as output voltage decreases.

2.3. Class-AB Amplifiers

Fig. 3 shows that same output stage biased as class-AB. For small Vi, both devices conduct as in class-A. For large Vi, one device is on and the other off as in class-B. For the price of a small quiescent current, the dead zone and crossover distortion is eliminated.

Average power supply current is

$\overline{I_S}(\Theta_Q) = \frac{I_{L_{\max}}}{\pi}\Theta_Q \sin\Theta_Q + \frac{I_L}{\pi}\cos\Theta_Q$ where $\Theta_Q = \sin^{-1}(2I_Q / I_{L_{\max}})$, as shown in Fig. 3, is the transition angle between class-A and class-B operation. The extreme values of Θ_Q are 0 and $\pi/2$, corresponding to the class-B and class-A operating points, with average supply currents of $\frac{I_L}{\pi}$ and $\frac{I_{L\max}}{2}$ respectively. The average supply power is then

$$P_S = \frac{2V_{L_{\max}}}{\pi R_L}\left[1 + \frac{V_{DS_{sat}}}{V_{L_{\max}}}\right](V_{L_{\max}}\Theta_Q \sin\Theta_Q + V_L\cos\Theta_Q)$$

and the expression for efficiency is [16]

$$\eta = \frac{\pi}{4}\frac{V_L}{V_{L_{\max}}}\frac{1}{1 + R_{DS_{on}}/R_L}\frac{V_L/V_{L_{\max}}}{\Theta_Q \sin\Theta_Q + (V_L/V_{L_{\max}})\cos\Theta_Q}$$

For a full-scale input, efficiency ranges between about 50 and 76%. With Θ_Q of $\pi/8$ (which has been used for the amplifier described in this paper), efficiency at full scale is about 68%. Full speaker power might be too loud for many listening situations. A more common listening level might be 40% of full-scale, at which point efficiency ranges between 20 and 50%, and about 38% for $\Theta_Q = \pi/8$.

2.4. Analog Class-D Amplifiers

Class-D amplification solves the efficiency problem. Fig. 4 shows a class-D output stage [14]. (The input and power-output signals are only representative pulse width modulation and do not correlate to the sinusoidal output.) The LC low-pass filter reconstructs the analog output, which is the moving average of the input signal. MP and MN act as switches, so that the power waveform (at their drains) swings from VDD to VSS. Ideally, MP and MN have zero on-resistance and infinite off-resistance and thus dissipate zero power whether off or on. Likewise, no power is dissipated in the reactive LC filter so ideally all of the input power is dissipated in the speaker for 100% efficiency, regardless of the output power level.

In an all-analog class-D amplifier, the PWM pulse train is obtained from a comparator with the low-power audio signal as one input and a triangle or sawtooth wave as the other input as in Fig. 5 [4].

In this example the audio signal is compared to a triangle wave, and the running average voltage of the output PWM stream is proportional to the input SIG. The comparator operates continuously. Its output can change state at any time. This type of system has been named natural pulse-width modulation, (NPWM). The following is a list of non-idealities of an NPWM system that degrade performance [17,18].

1. Finite switching times change pulse widths from their ideal, and these width changes are asymmetrical since the switching-times of P- and N-channel MOSFETs are different and don't necessarily track well.

2. The amplitude of the output pulse depends upon the speaker load, especially during rising slopes of the analog signal.

3. High-frequency ripple can change the slicing level of the comparator, causing pulse-width errors.

4. Overshoot and ringing in the PWM signal due to layout and de-coupling problems, and common impedance paths.

5. Vanishing pulses if short (or long) compared with switching time.

6. Power supply ripple causes pulse-to-pulse amplitude error, which produces audible tones.

7. LC filters can be can be difficult to design when required to work over a large variation of loudspeaker impedances. Cost of such a filter may be large if these components are not to add distortion in the signal path (e.g. inductor saturation)

2.5. Digital Class-D Amplifiers And PWM - D/A Converters

The straightforward digital counterpart to all analog PWM is to make a digital comparison between a digital triangle-wave and a stream of digital samples of a signal. Equivalently, one could simply load the sequence of samples into a counter that triggers the pulse edge when the count reaches zero. In either case, the pulse edges occur only at discrete time points rather than in continuous-time. Restricting pulse transitions to multiples of a clock interval has been named uniform pulse-width modulation, (UPWM). The errors of UPWM add to the errors of the PWM output stage listed above. Research has

been done through the years to eliminate or reduce the effects of these non-idealities [12].

The input sequence of pulse-code modulation (PCM) words are converted to a PWM bit-stream that drives the class-D output stage. For acceptable performance it is necessary to overcome distortion-causing errors due to UPWM. Digital signal processing can compensate for timing errors, and delta-sigma noise shaping can enable the use of lower clock frequencies.

Fig. 6 is a block diagram of a PWM DAC/Class-D Amplifier [14].

The oversampling filter, cross-point detector and noise-shaping filter reduce the number of bits into the pulse width modulator without excessively increasing quantization noise and distortion. The required clock frequency for the full resolution of the digital input would be too high otherwise.

The oversampling filter interpolates zero-samples between input samples and filters the result. The output is clocked at some multiple of the input frequency, for instance, raising the sampling frequency from 44.1 to 176.4 kHz, and is followed by a digital filter. Linear or non-linear DSP algorithms in the cross-point detector result in a compromise between natural and uniform sampling that reduces distortion. The design of the cross-point detector has been a rich area for research. Examples in the literature range from simple and crude to very complex – some requiring a dedicated DSP integrated circuit.

The noise-shaping filter reduces the number of input bits into the PWM and shapes the increased quantization noise out of the audio band. This reduces the required time resolution of the system. For example, consider a 16-bit signal sampled at 44.1 kHz interpolated and up-sampled to 352.8 kHz (for a period of 2.8 us). Sixteen bits would result in two to the sixteenth or 65536 distinct pulse widths. Thus the down counter clock would need to run at 65536 * 352.8 kHz = 23 GHz (for a period of 43 ps). DSM noise shaping can be used to reduce the number of bits and therefore the clock rate.

A passive LC filter, typically fourth order, removes the high frequency components from the power signal.

Problems remaining with digital PWM systems [17,18]:

- Error correction to reduce the non-idealities of UPWM (in comparison to continuous-time NPWM) is computationally intensive.
- Excess out-of-band noise, as shaped by delta sigma modulation, must be removed by passive LC filter. In addition, large out of band noise may remix with other clocks in the system resulting in the folding of the shaped noise into the baseband audio signal.
- Even with bit reduction by delta-sigma modulation, the clock frequency of the counter is still very high for a full-bandwidth system in comparison to continuous-time NPWM.

From the above it can be seen that increasing efficiency by means of class-D is difficult and expensive if the performance attributes are to be comparable to a class-AB amplifier. The goal is to increase efficiency cheaply and robustly without sacrificing audio quality.

3. PWM-PAMP

Three major disadvantages of the fully digital PWM DAC are:

1. The added complexity of pre-compensating the PWM sequence, requiring an external dedicated digital signal-processing IC for best performance.
2. The increased power dissipation due to high clock rate.
3. The electromagnetic interference emitted by the power devices switching at this high clock speed.

Furthermore, there is still significant residual harmonic distortion [13].

To eliminate these disadvantages, the PWM-PAMP uses a much simpler scheme, in which a class-AB fully differential output stage is powered by voltage rails that track the output voltage, keeping the driving transistors in the saturation region, but with only minimum overdrive. These voltage rails are the outputs from a simplest UPWM D/A converter.

1. This PWM DAC can be extremely simple and small because larger quantization error is acceptable, and therefore only 7-8 bits need be decoded.
2. It can operate at comparatively low clock rates, once again because larger distortion on the power rails is tolerable.
3. It takes advantage of the inherent power supply rejection of the fully differential class-AB amplifier to eliminate the effect of

residual ripple and high frequency out of band noise on the power rails. Thus no LC filters are required at the output of the amplifier.

4. The LC filters at the PWM rails do not have the stringent THD requirements that exist for a class-D amplifier, for driving loads with a high current.

The concept of tracking power supply rails using continuous time PWM tracking rails has been disclosed in a 1998 Patent [19]. The complexity of implementing a tracking power supply system fully in the analog domain can be seen in the extensive and detailed drawing which are part of this patent.

3.1. PWM-PAMP Output Stage

Fig. 7 shows a top-level block diagram of the PWM-PAMP system, including the Audio DAC, digital delay, 4-output PWM, power rail switches, passive filters, and the class-AB power amplifier. In this system, a differential class-AB output stage is used to double the effective rail voltage, which is a significant issue in designing fully integrated amplifiers that operate at low voltage, such as the 3-Volt system simulated for this article. Description of the system begins at the output. The differential class-AB output stage of the PWM-PAMP is shown in Fig. 8. PWM pulse trains are processed by break-before-make logic. Their drive strength is increased and applied to the gates of the power switches. The power switches apply VDD or VSS to the inductors. The LC network filters the pulse trains into continuous time analog signals that track but are offset from the differential audio signal. The offsets are enough to keep the driving transistors in saturation when they are in the conducting mode of the AB process. The power supply rejection of the output stage can tolerate significant distortion on the four supply waveforms – Vdp, Vsp, Vdn and Vsn. The bold lines in Fig. 8 indicate the current path during a large positive output swing.

The output and tracking power rail waveforms are shown in Fig. 9. For a typical differential class-AB amplifier, Vn = -Vp, Vdp (max) = Vdn (max) = VDD, and Vsp (min) = Vsn (min) = VSS. For the PWM-PAMP, Vn = -Vp. Vdp and Vsp have the same amplitude and phase as Vp, and are offset above and below Vp. Similarly, Vdn and Vsn have the same amplitude and phase as Vn, and are offset above and below Vn. These DC offsets are enough to keep all four driving transistors in saturation. The power supply rejection of the operational amplifier can tolerate significant distortion on the four supply waveforms – Vdp, Vsp, Vdn and Vsn.

3.2. Input Digital Signal And Audio DAC

The input to the system is a 16-bit pulse-code modulated signal at 44.1 kHz sampling rate. All sixteen bits are input to an audio DAC.

3.3. Pulse-Width Modulator

The audio signal's eight most significant signal bits are input to the pulse width modulator, over-sampled by four by zero-order hold, resulting in sinc filtering. The 4X upsampling removes spurious components of 44.1 and 88.2 kHz. An 8-bit UPWM rate of 256 * 176 kHz = 45.5 MHz. Fig. 10 is a block diagram of the pulse width modulator. The Data Latch stores the eight MSBs of the digital input signal. This latch is clocked at a 45.5 MHz rate, but the Counter reads in the data with the 176 kHz LOAD.

COUNT is the digital state of the counter. When LOAD is active, the input data bits load into COUNT on the next CLOCK pulse. On subsequent CLOCK pulses, COUNT reduces by one. There are four trigger values and four output lines. While COUNT is equal to a trigger value, the corresponding output line is asserted. The TRIG lines go to four pulse formers.

The PULSER state machines operate on the edges of TRIG and CLOCK and depend upon their previous state as well as the LOAD input. When LOAD is active, the next edge of CLOCK creates the active edge of output PWM. When PWM is active, a rising edge on TRIG creates the trailing edge of PWM.

Trigger levels and output polarities of the four PULSER blocks are chosen for the desired phase and offset of the tracking rails. There is also a control input that disables the pulse width modulator. When disabled, the power rails go to the normal power rails, VDD and VSS.

The tracking rails are aligned with the DAC output by means of the digital delay block. If the tracking rails were not carefully aligned to the phase of the signal being amplified by the power amplifier in the main signal path the head room between one tracking rail and the output would be reduced resulting in increased distortion. The effect becomes more significant as the frequency of the input signal is increased.

3.4. PWM Switch And Passive Filter

A "break-before-make" switch is constructed from logic gates and switching transistors. Ideally, the devices that switch between the power rail and ground to couple the PWM signal to the low pass filter would have infinite off resistance and zero on resistance. To approximate this ideal, transistors with large width-to-length ratios are used for the switching devices. The large gate capacitance of the switching transistors necessitates a chain of inverters of increasing drive strength. To create the break-before-make attribute, the signal controlling the P-FET switch rises before, and falls after the signal controlling the N-FET switch. Thus, the P-FET is in the off state before the N-FET turns on, and vice versa. Logic gates and a delay chain of inverters accomplish this. The switching devices are protected by diodes from over-voltages due to switching large inductor currents on and off.

Each of the four signals PWM[3:0] is thus stepped up in drive power and applied to a switch that connects either VDD or VSS to a passive LC low-pass filter. The outputs of these filters are the four tracking power voltages – Vdp, Vsp, Vdn and Vsn that power the output stage of the audio power amplifier.

3.5. Audio DAC

All sixteen bits of the digital signal and the 44.1 kHz clock (LOADN) go to an audio DAC. The architecture, design and performance of the audio DAC are not discussed in this article. An ideal DAC model was used for simulation purposes. The differential voltage waveforms from the DAC are input to the smoothing filter and power amplifier.

3.6. Smoothing Filter And Class-AB Driver

Fig. 11 shows a block diagram of the power amplifier and smoothing filter. The DC feedback path for common mode control is not included.

The smoothing filter removes the high frequency components from the zero order hold output from the DAC. This configuration can provide fixed gain or with variable resistances can provide programmable attenuation or gain. The input differential pair and second (gain) stage are not shown or analyzed here. The output stage is of more interest and will be discussed in some detail.

The output stage can be analyzed and an expression derived with which to estimate efficiency. The highlighted current path shown earlier in Fig. 8 shows the flow for a strong positive VOP, in the Class-B State. Total power dissipation is the power delivered to the load, plus the class-AB current times the constant VDS, plus that current squared times RDS on of the switches. That is, $P_S = P_{Load} + P_{AB} + P_{SW}$. Power delivered to the load is as usual, $P_L = V_L^2 / R_L$. Class-AB current, taking Θ_Q into account, is $I_{AB} = \frac{V_{L_{\max}}}{\pi R_L}\Theta_Q \sin\Theta_Q + \frac{V_L}{\pi R_L}\cos\Theta_Q$. The key feature of this system is that VDS is kept constant (neglecting ripple on the tracking rail). Assume constant VDS for both N and P FETs to get the expression for power dissipated. $P_{AB} = \frac{V_{DS}V_{L_{\max}}}{\pi R_L}\Theta_Q \sin\Theta_Q + \frac{V_{DS}V_L}{\pi R_L}\cos\Theta_Q$.

The power dissipated by the PWM switches is $P_{sw} = I_{AB}^2 R_{DS_{SW}}$. Assume identical switch resistance for the P and N FETs, and ignore leakage in the off state. The expression for power supply power dissipation is given at the bottom of the page.

Efficiency is once again the power delivered to the load divided by total power dissipated. Fig. 12 is a graph of predicted efficiency versus output level for various values of Θ_Q.

Compare this to the predicted efficiency of a class-AB output stage with fixed DC rails shown in Fig. 13 [16.].

$$P_S = \frac{V_L^2}{R_L} + \frac{V_{DS}V_{L_{\max}}}{\pi R_L}\Theta_Q \sin\Theta_Q + \frac{V_{DS}V_L}{\pi R_L}\cos\Theta_Q \ldots$$

$$+ R_{DS_{SW}}\left[\left(\frac{V_{L_{\max}}}{\pi R_L}\Theta_Q\right)^2 \sin^2\Theta_Q + \left(\frac{V_L}{\pi R_L}\right)^2 \cos^2\Theta_Q + V_L V_{L_{\max}}\left(\frac{\Theta_Q}{\pi R_L}\right)^2 \sin\Theta_Q \cos\Theta_Q\right]$$

4. SYSTEM MODEL AND SIMULATION TEST BENCH

This section describes the modeling, simulation and evaluation of the system. The main design tool set is the Cadence mixed signal integrated circuit design package. The system and test bench was defined in schematic form with the Composer tool. The overall simulation engine is the Cadence AMS (analog and mixed signal) simulator. This simulator engine calls and arbitrates control between the following specialized simulators:

- Spectre simulates the electrical behavior of transistor and passive device models as well as behavioral models of larger blocks written in the Verilog-AMS language. Fourier analysis following a transient simulation is available with this simulator.
- NCSIM simulates Verilog models of digital circuits, behavioral, RTL and structural (netlists of gates). It is a very fast event-driven simulator.
- SimVision is the waveform display tool that includes some post-processing abilities.

Matlab was used, both early in the design phase and for the final analysis phase. Simulink, the graphical interface to Matlab, was used to develop the system concept of the PWM-PAMP. The final plots of derived numerical results from the post-processed simulation results were plotted with Matlab.

The data latch, counter and pulser comprising the pulse width modulator were modeled as synthesizable RTL Verilog. Continuous time values of analog voltages and currents were important for the power switching FETs as well as their preceding inverter string and the break-before-make logic, so this circuitry was modeled at the device level and simulated with Spectre under AMS control. The LC filters as well as the entire power amplifier were also modeled at the device level and simulated with Spectre. The audio DAC was modeled behaviorally with Verilog-AMS.

This collection of models of the PWM-PAMP system was embedded into a test circuit that was stimulated and evaluated by the AMS simulator. The simulation test bench includes digital and analog behavioral models to drive and monitor the system. Overall simulation-control, clocking, and generation of digital control signals was implemented with digital behavioral models written in the Verilog language.

Analog and mixed-signal behavioral Verilog-AMS models were developed to

- Create the digital signal from an analog independent sine source by means of an ideal A/D converter.
- Create power probe devices.

- Power probes are connected at various places in the schematic and model an infinite impedance voltmeter across, and a zero impedance ammeter in series with an element whose power dissipation is of interest. The voltage output waveform from the power probe is proportional to the instantaneous power: $\mathrm{Vout} = \mathrm{Vin} \cdot \mathrm{Iin} \cdot 1\mathrm{Volt/Watt}$. The SimVision waveform display tool is used to post process the waveform and calculate average power dissipation during a defined interval.

5. SIMULATED RESULTS

A suite of simulations were performed to evaluate:

1. Signal to distortion ratio (SDR) as a function of output amplitude for two frequencies.
2. Efficiency as a function of output amplitude for two frequencies.
3. Frequency response for two fixed amplitudes.
4. Efficiency as a function of frequency for two amplitudes.

This suite was run with two test benches – one using the PWM tracking rails, and the other using DC rails.

Simulated results comparing SDR versus amplitude at 1 and 4 kHz for DC and PWM tracking rails can be seen in Fig. 14 and Fig. 15. The 0-dB full-scale output level is arbitrarily defined as 3V p-p differential over a 30-Ohm load. The performance with PWM tracking rails is comparable to that of the traditional class-AB amplifier up to about +3dB full scale.

Simulated results comparing efficiency versus amplitude are shown in Fig. 16. About an 8% increase in efficiency can be seen down to less than half-power. This could be improved with larger power supply voltages. Fig. 17 shows frequency response at full scale and –4 dBfs with PWM and full scale with DC rails. Notice that the PWM and DC rail frequency response graphs nearly overlay. Fig. 18 shows efficiency as a function of frequency for full scale DC and for full scale and –4 dBfs with PWM rails. The PWM-PAMP system is more efficient up to 10 kHz.

6. HARDWARE PROTOTYPE

A prototype system from discrete components proves the PWM-PAMP concept using a single ended amplifier with 12-Volt supplies. See Fig. 19.

Digital audio signals from a CD player are input as S/PDIF data to the Crystal Semiconductor Emulation Board. The Crystal Emulation includes a D/A converter that creates the analog signal sent to the discrete op amp, and also provides the digital signal, which goes to controller.

The controller interfaces the audio data from the Crystal Emulation Board (CDB4334) to the pulse width modulator circuit, converting the data from two's complement to offset binary format. A data delay aligns the digital data signal to the analog signal from the Crystal Board's D/A converter.

The digital portion of the PWM circuit was implemented using a Xilinx XC2S50 FPGA, a low-cost FPGA that can implement up to about 50,000 equivalent logic gates. The PWM circuit loads the audio data from the controller circuit, and counts down to trigger levels to generate the pulse stream. The PWM circuit outputs pulse-width modulated signals for the upper and lower power-rails of the amplifier.

The FPGA was programmed using the Xilinx Foundation ISE software, which compiles synthesizable Verilog HDL files into a programming file that is downloaded into the FPGA. The Verilog input describing the PWM circuit and associated control consists of approximately 300 lines of code. The logic compiled from this input consumes about 25% of the capacity of the XC2S50 FPGA.

The prototype has some limitations. The 4X-oversampling rate is not available from the Crystal emulation board. The signal sampling rate into the PWM is therefore 44.1 rather than 176 ks/s, and the PWM clock frequency is 11.5 rather than 45.5 MHz. The UPWM scheme used is slightly different from that of the simulated system, again because of the available functions within the FPGA. The lower PWM bit rate necessitated a lower frequency reconstruction filter, since the incoming signal contains spectral components at 44.1 and 88.2 kHz (that are eliminated by the 4X up-sampling), which must be rejected by the analog LC filter. For ease of assembly and flexibility for experimentation, active filters were used instead of LC filters. The filters were 4th order Butterworth with corner frequency at 10KHz. Their phase shift becomes significant enough to misalign the tracking rails from the signal at about 5 kHz. Thus the audio bandwidth of the prototype was limited to about 5 kHz. Since the tracking rails are powering a discrete op amp, and not just the driving stage of a class-AB amplifier, the headroom of the op amp limits the VDD –Vsig, and Vsig – VSS potentials.

Figs. 20-23 were constructed from oscilloscope plots of outputs and PWM tracking rails. Fig. 20 shows a 400 Hz tone burst output with the associated tracking rails. The tone burst allows the reader to see the DC levels associated with the tracking rails and output signal. Fig. 21 shows greater details of a 1 kHz sinusoid output and its tracking rails. Fig. 22 shows a 5 kHz sinusoid and its associated tracking rails. Fig. 23 shows a 1 kHz square wave output and its associated tracking rails. Note the rise and fall times of the tracking rails are sufficient to stay above/below the output signal. The truncation of harmonics in the D/A converter on the Crystal emulation board results in the visible ripple in the output signal. The expected overshoot for a 4^{th} order Butterworth filter can be seen in the tracking rails. Note that the tracking rails transition at sufficiently fast rate that the leading edge of the output of the amplifier after the transition has all expected ripples which would be missing if the op amp had be driven into a non linear mode of operation during the transition.

For these tests, there was built-in headroom of 1.5 Volts on the positive rail and 1.2 Volts on the negative rail that may not have been necessary but was convenient for early runs of this prototype.

7. CONCLUSIONS

Black first described pulse-width modulation in 1953 [20]. An early application of PWM for improving power efficiency dates back to 1966 [3-5]. Disadvantages of class-D are its distortion, and the complexity and size that is required to reduce its distortion. Furthermore, high clock rates and very large DSP structures are needed to achieve reasonable audio quality.

This article described a PWM-PAMP system that compromises between efficiency, size and complexity and promises to be a workable, low-cost solution. A very simple digital PWM DAC creates tracking power rails for a fully differential class-AB amplifier. Low power, low voltage operation is possible because of the fully differential outputs. Efficiency is high first of all because of the class-AB operation, and second because of the nearly constant VDS over the driving transistors due to the tracking power rails. Only a relatively small number of digital gates are necessary for the digital PWM circuit. The

low quality of the PWM output is not important because of the power supply rejection of the amplifier's output stage.

A 3-Volt system was designed at the transistor and synthesizable RTL level and simulated with an advanced mixed-signal simulation engine. Simulations show only small degradation in signal to distortion ratio or frequency response within the system bandwidth, up to the amplifier's nominal full-scale output level. Efficiency was not as high as predicted analytically. This could be improved by optimizing the PWM power switches and the scaled drivers preceding them. At power supply levels over 3 Volts the efficiency of the PWM-PAMP versus a class-AB amplifier would stand out more.

A working hardware prototype using discrete components and an FPGA has been constructed that proves the tracking rail concept. This work potentially could lead to novel, well-performing, amplifiers for portable audio devices

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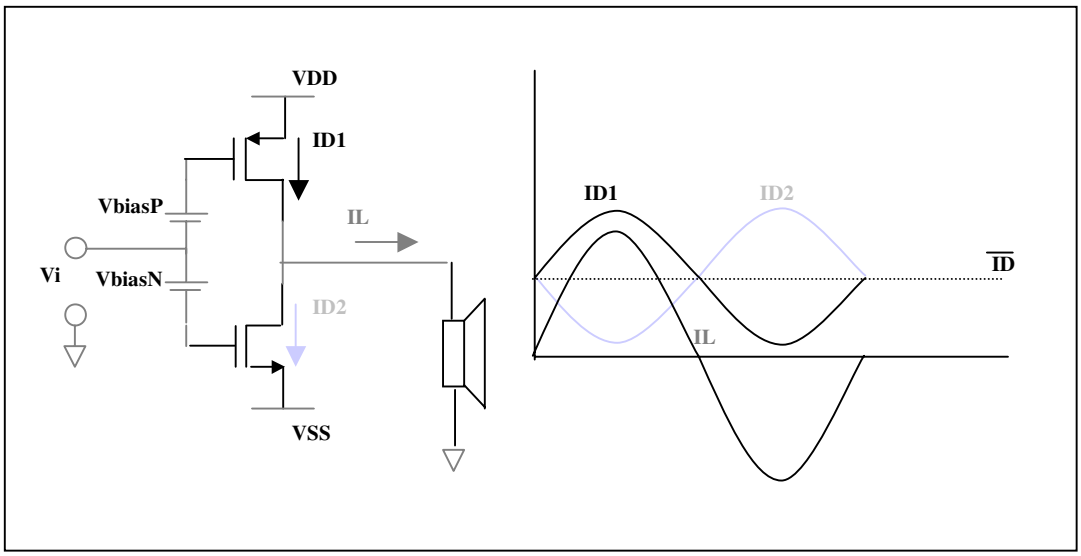

Fig. 1: Class-A Output Stage and Current Waveforms

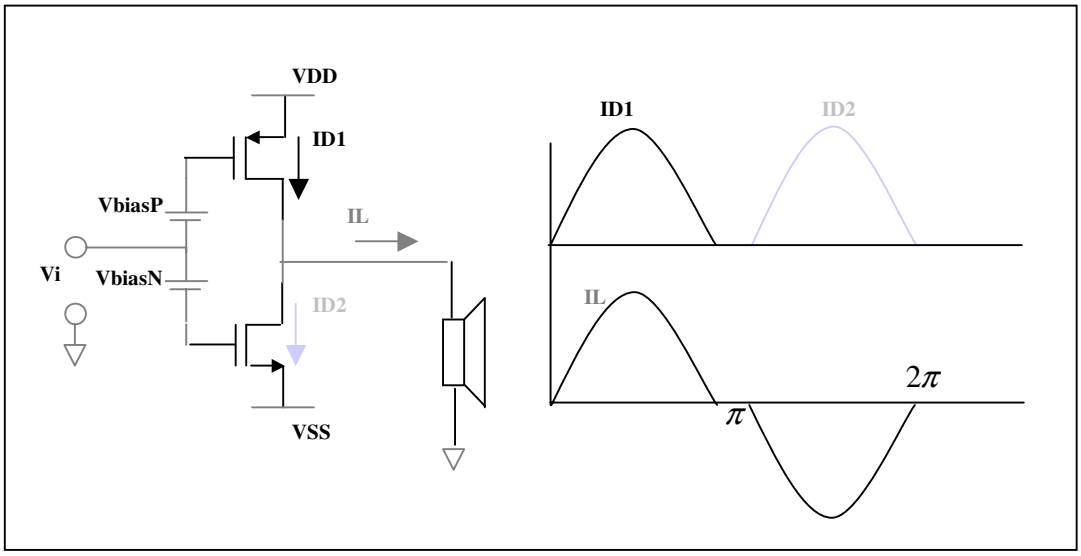

Fig. 2: Class-B Output Stage and Current Waveforms

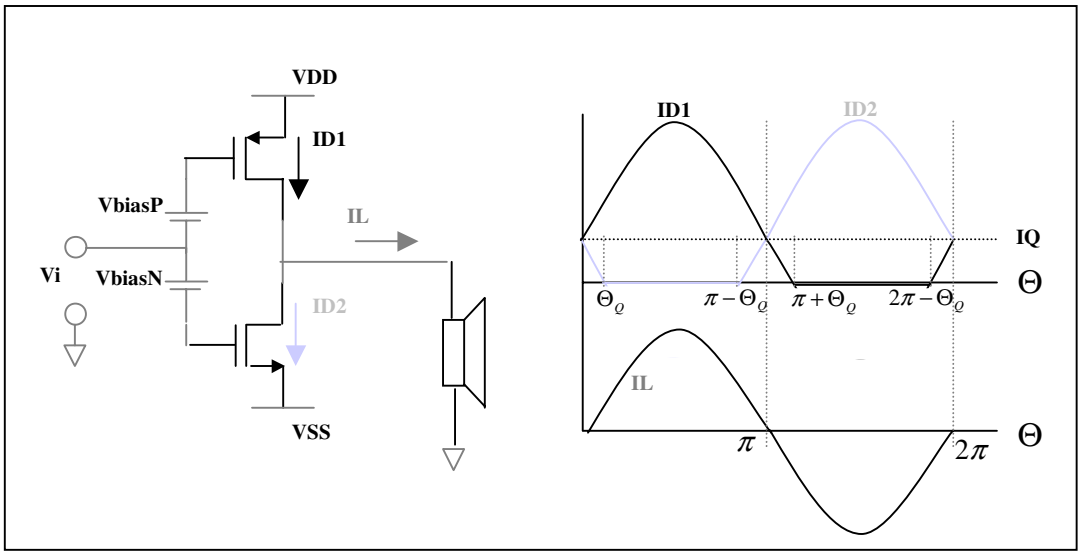

Fig. 3: Class-AB Output Stage and Current Waveforms

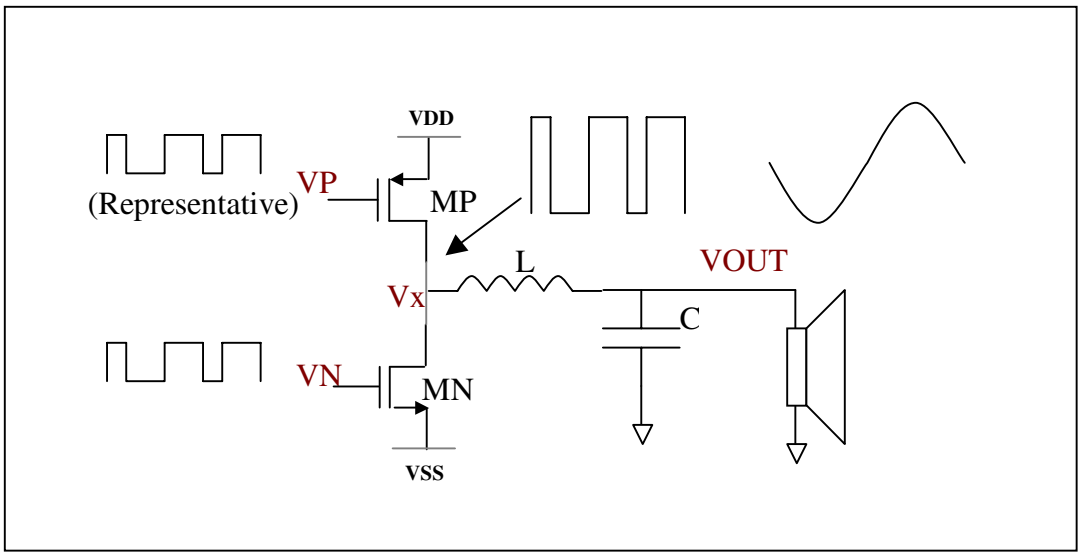

Fig. 4: Class-D Output Stage and Voltage Waveforms

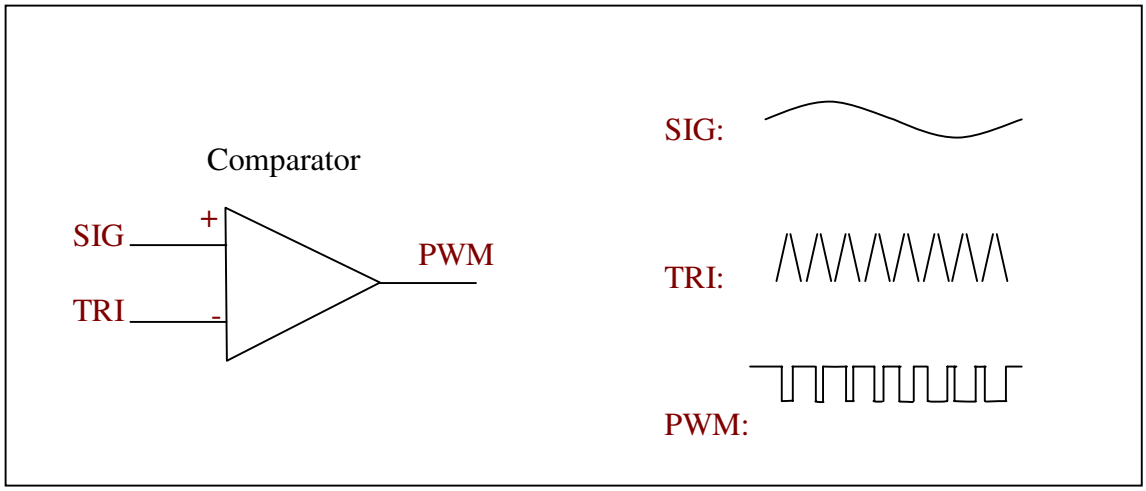

Fig. 5: Comparator and Waveforms for Analog Class-D

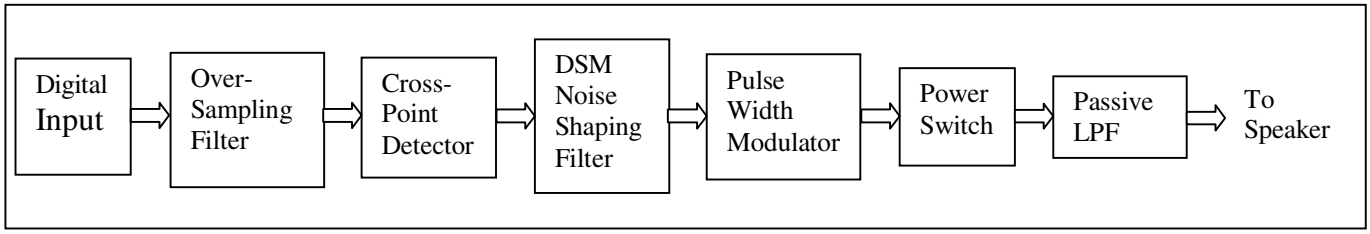

Fig. 6: PWM DAC/Class-D Amplifier

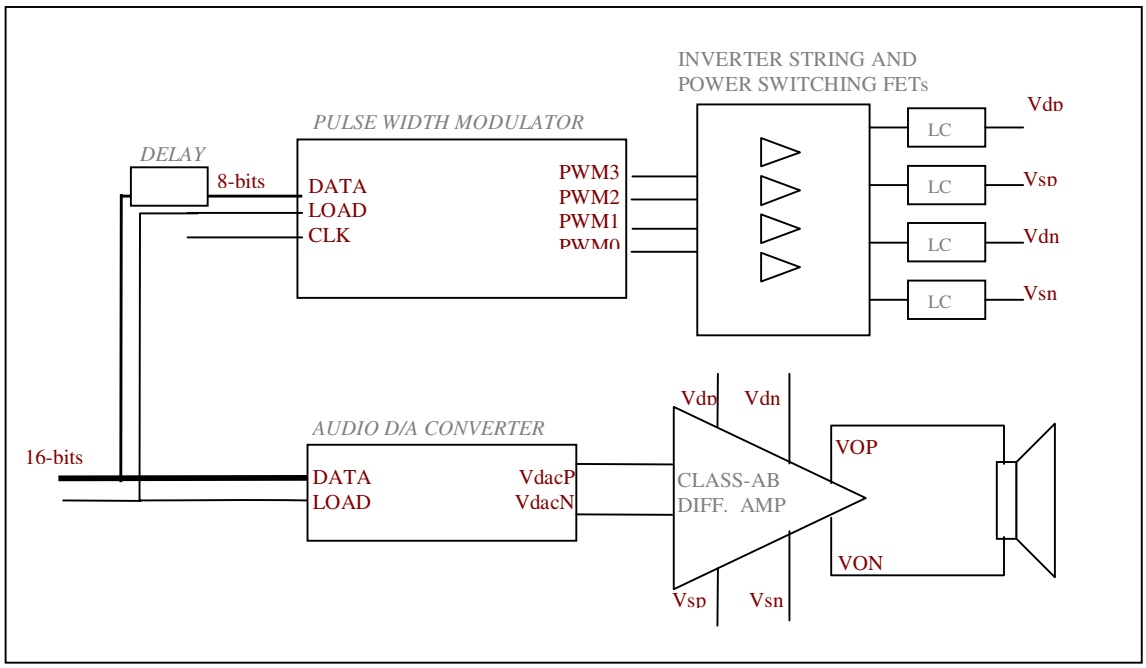

Fig. 7: Top Level Block Diagram of PWM-PAM

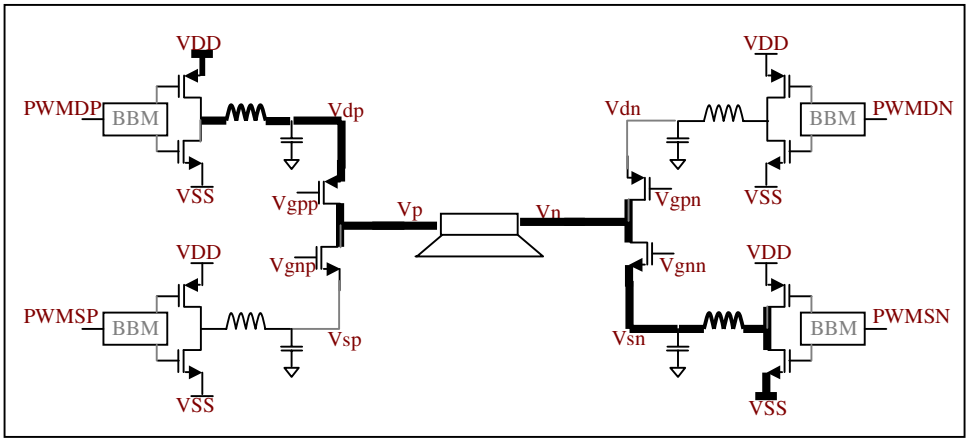

Fig. 8 : PWM-PAMP Output Stage

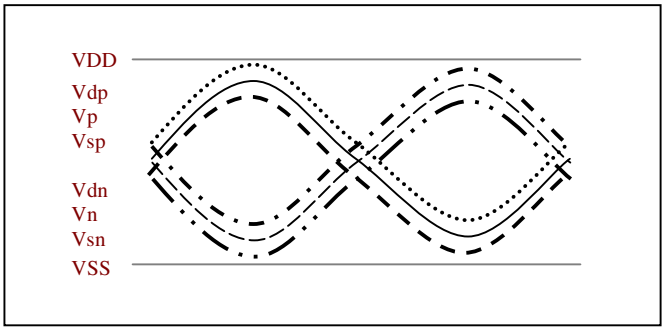

Fig. 9: Waveforms and Tracking Rails

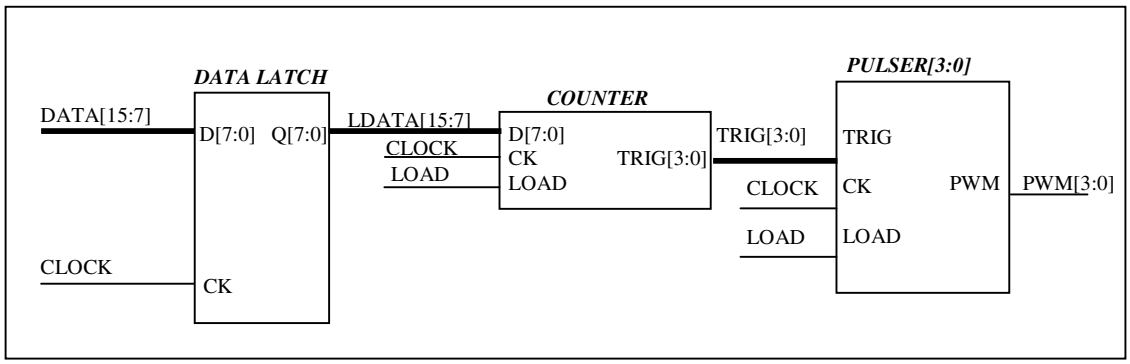

Fig. 10: Pulse Width Modulator Block Diagram

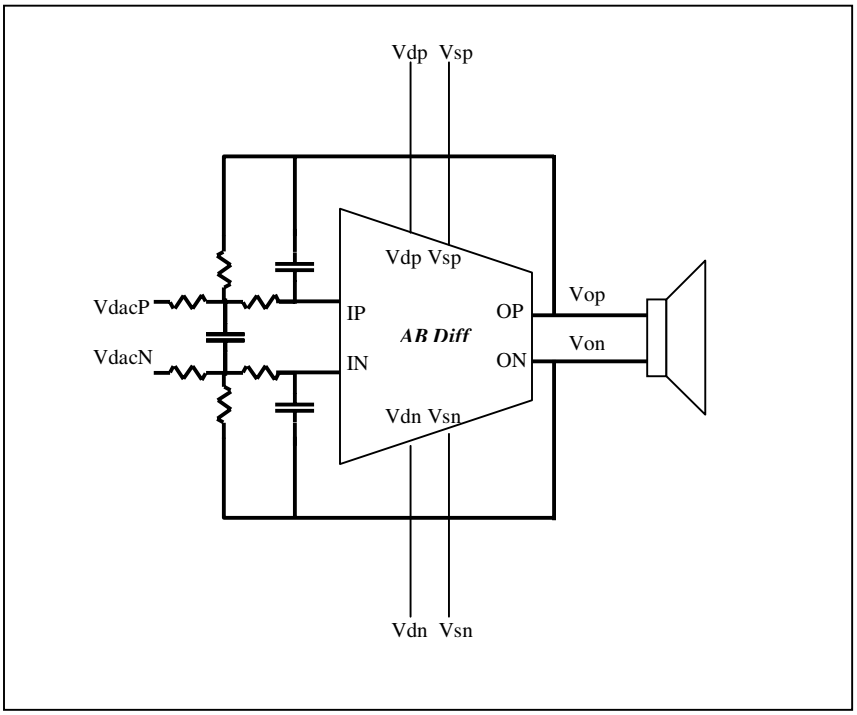

Fig. 11: Smoothing Filter and Power Amplifier

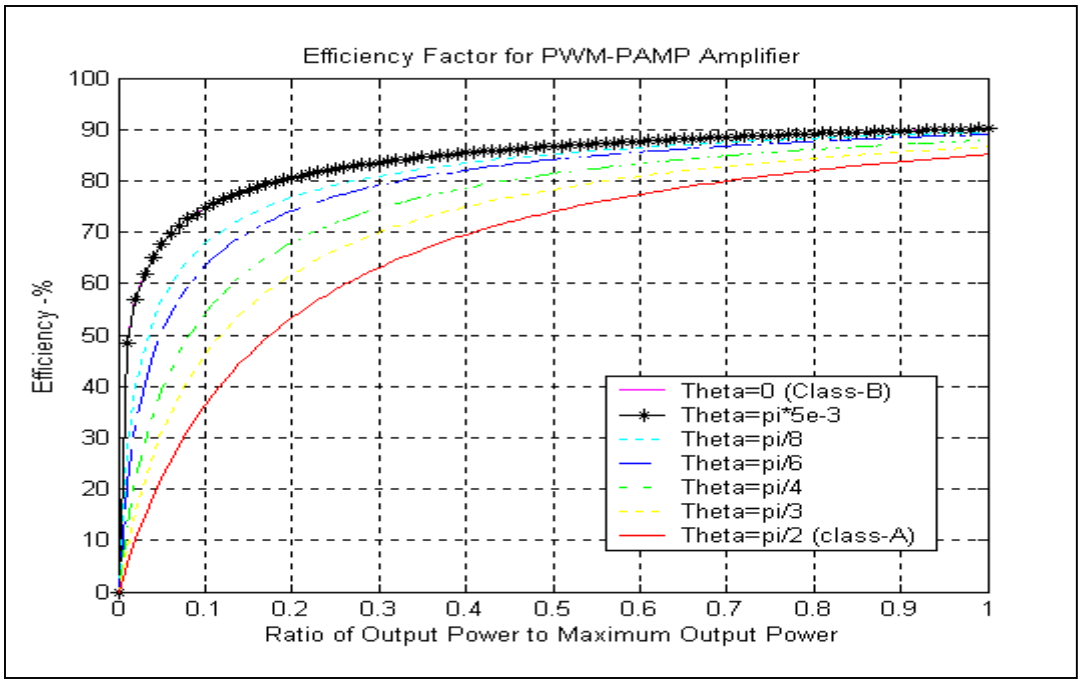

Fig. 12: Predicted Efficiency of PWM-PAMP. Theta = 0 and Theta = pi*5e-3 overlay each other.

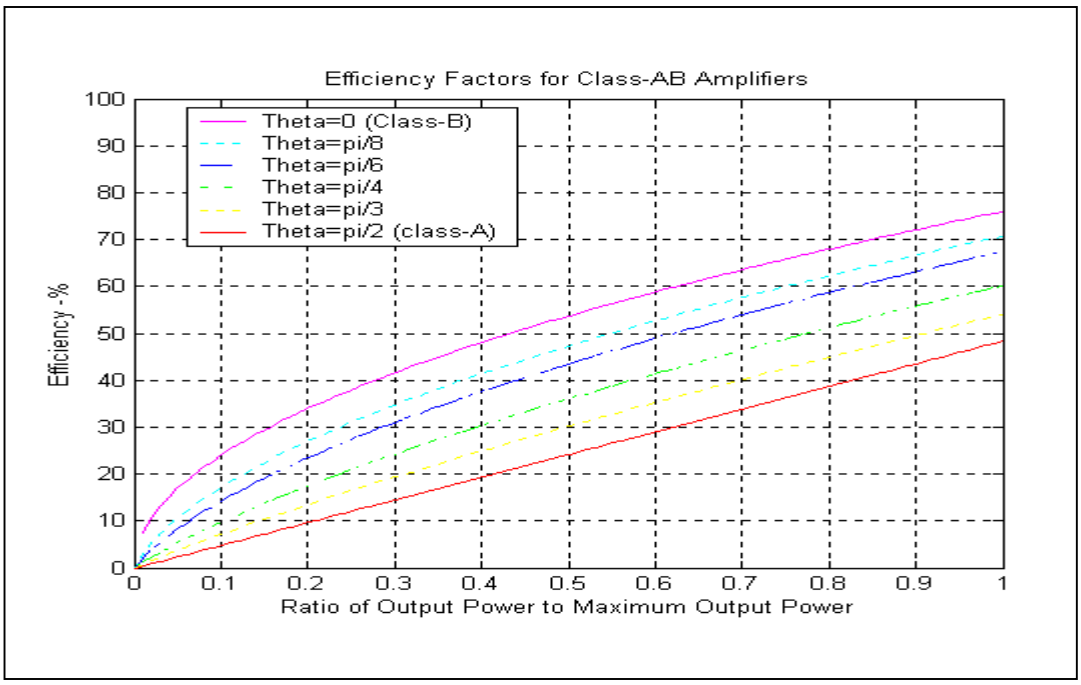

Fig. 13: Predicted Efficiency of Class-AB Amplifier

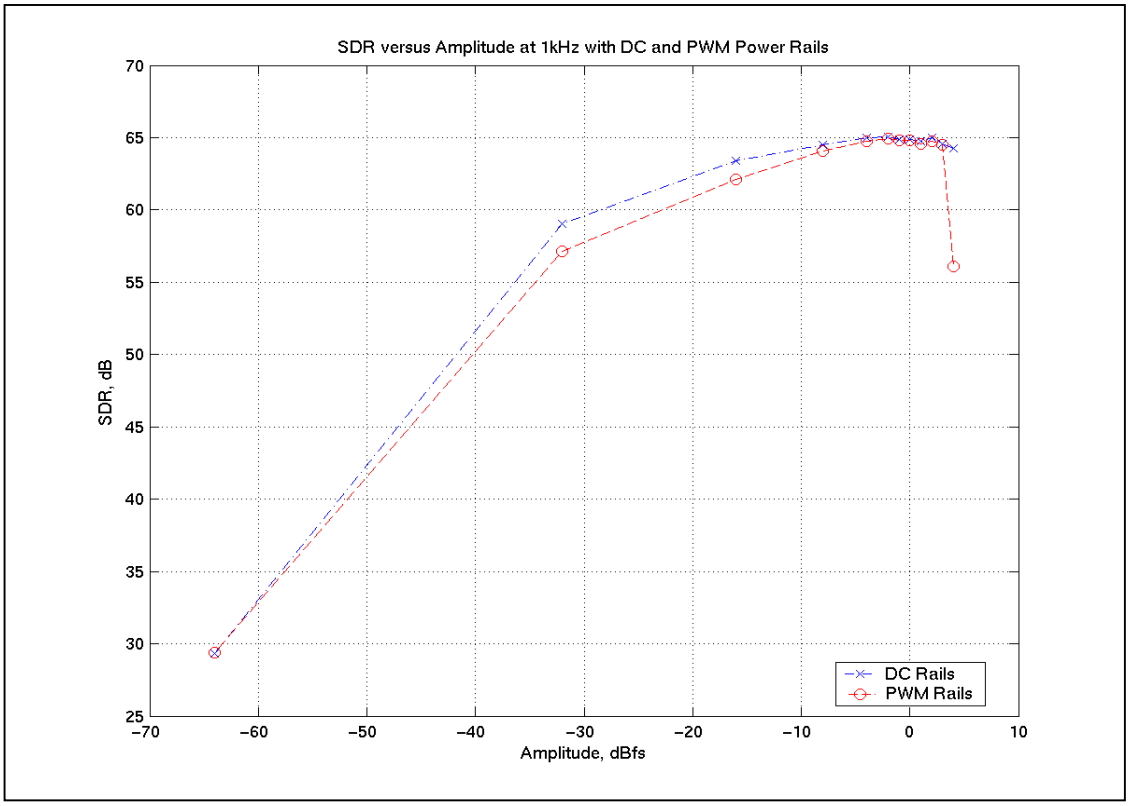

Fig. 15: SDR versus Amplitude at 1 kHz for DC and PWM

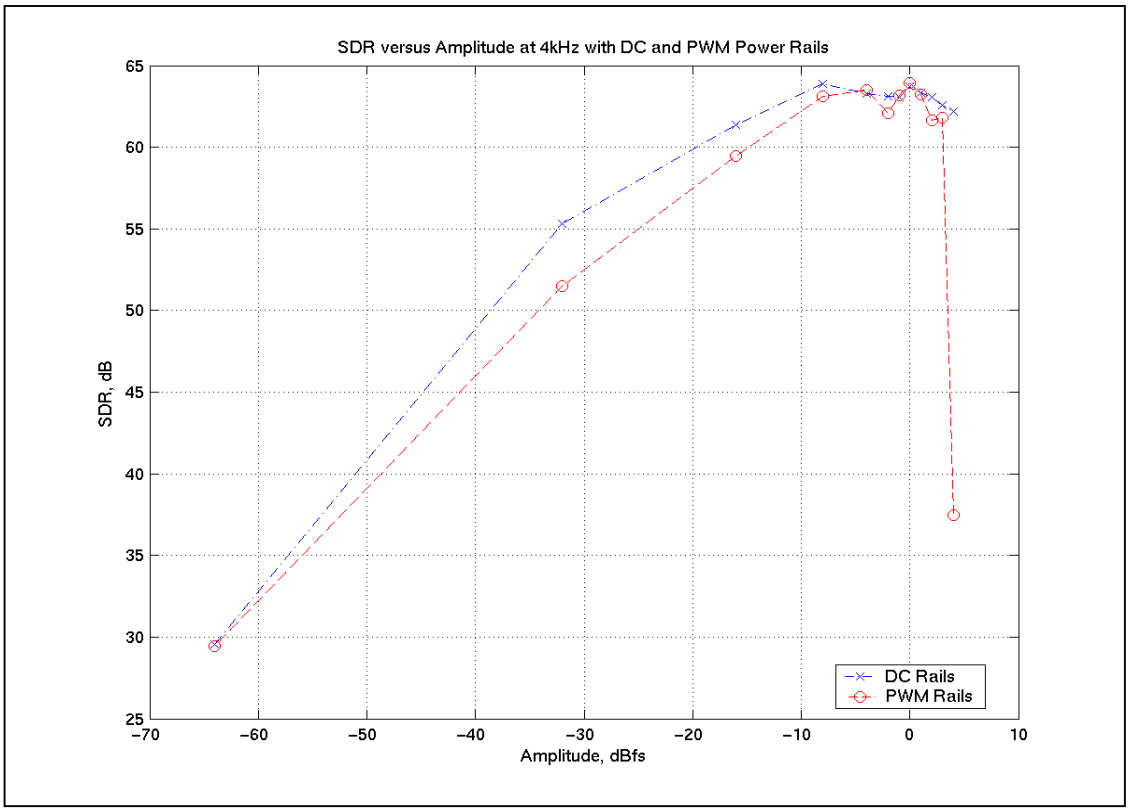

Fig. 14: SDR versus Amplitude at 4 kHz for DC and PWM

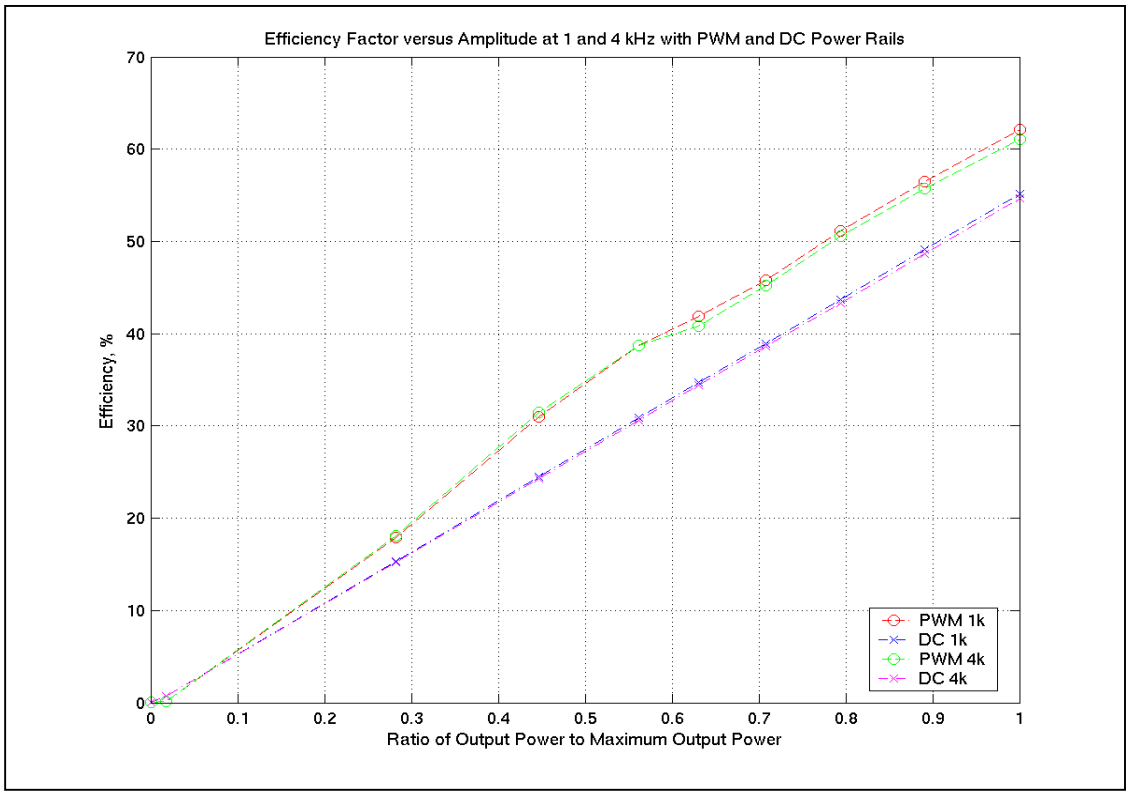

Fig. 16: Efficiency Comparison. 1 and 4k PWM traces overlay. 1 and 4k DC traces overlay.

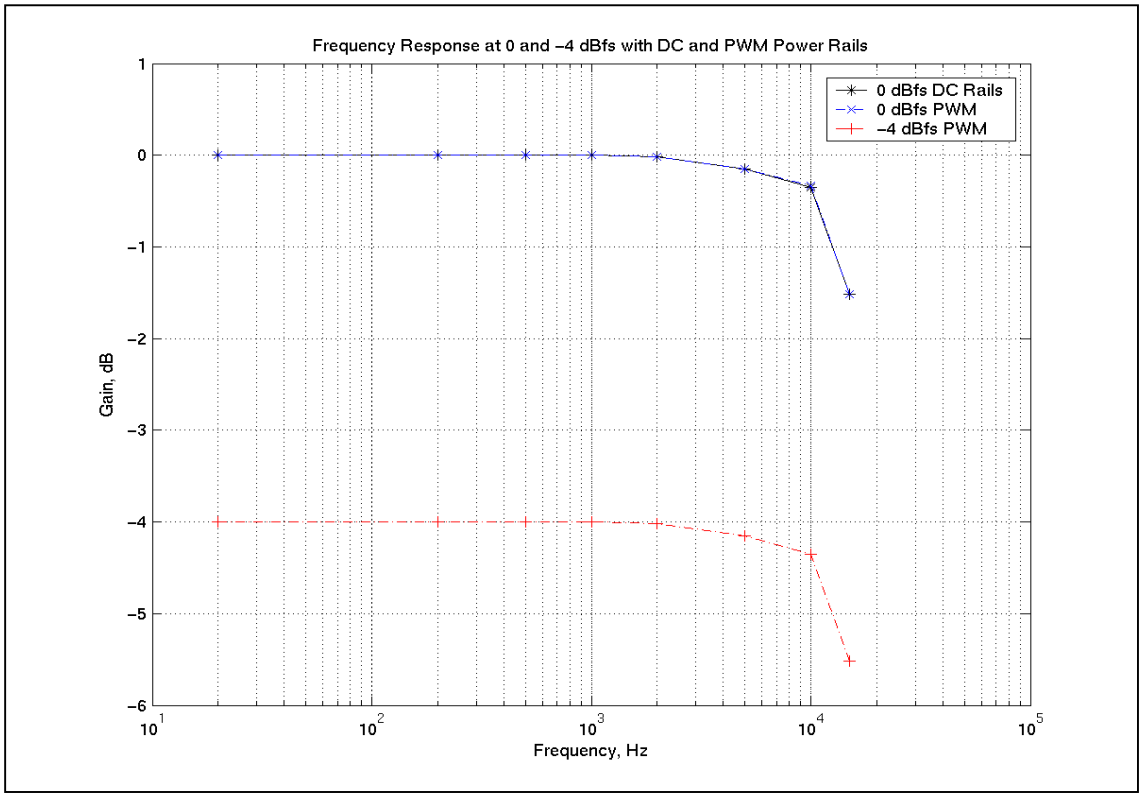

Fig. 17: Frequency Response. PWM and DC 0 dB traces overlay each other.

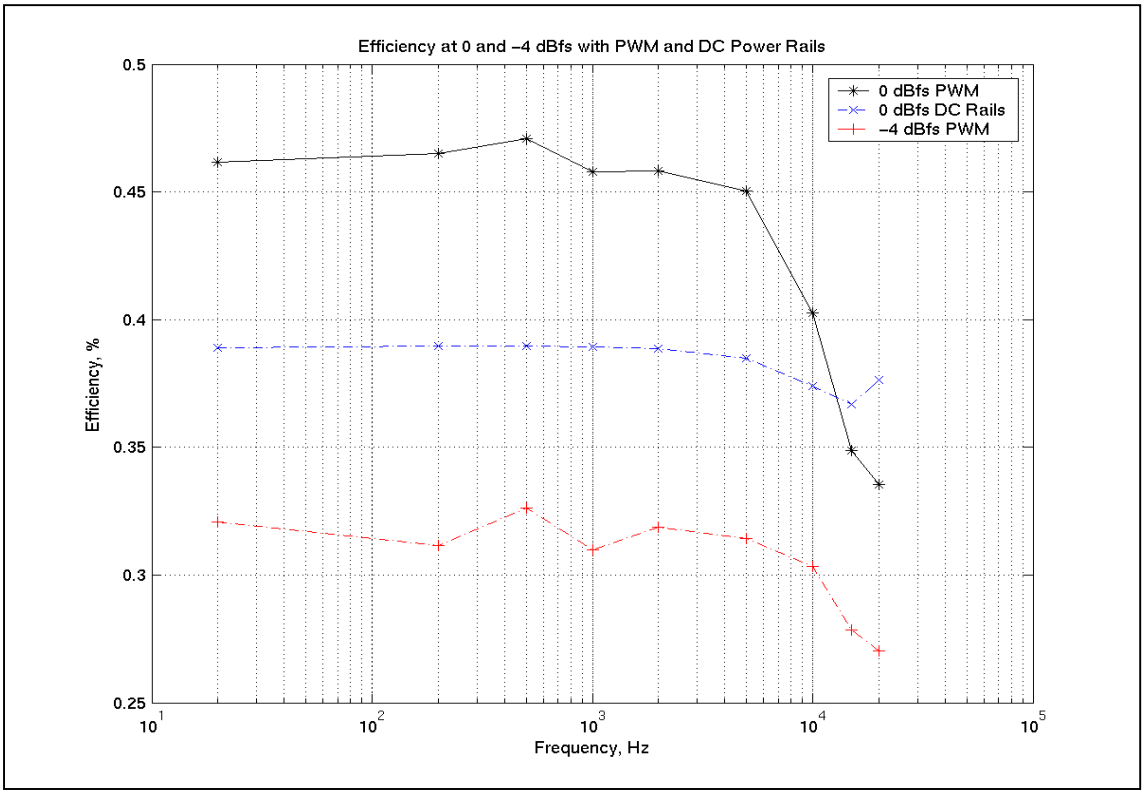

Fig. 18: Efficiency versus Frequency

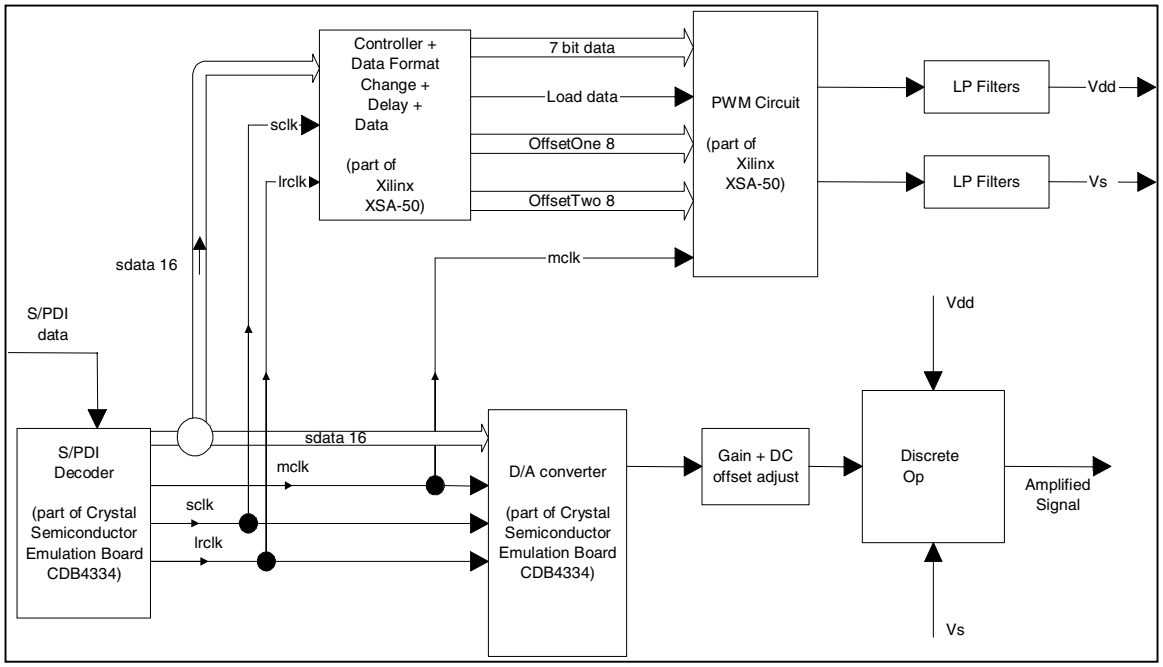

Fig. 19: Block Diagram of Hardware Prototype

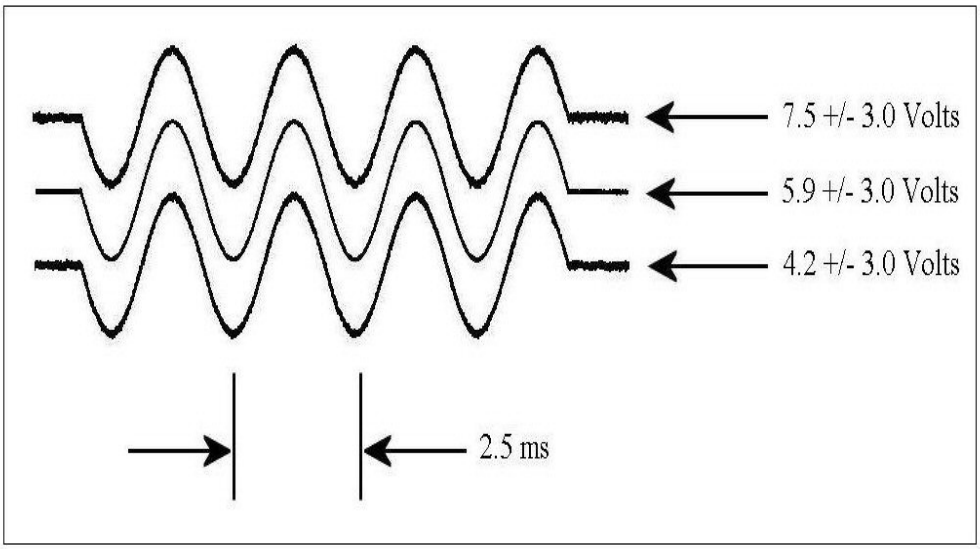

Fig. 20: 400 Hz Burst Output and Tracking Rails

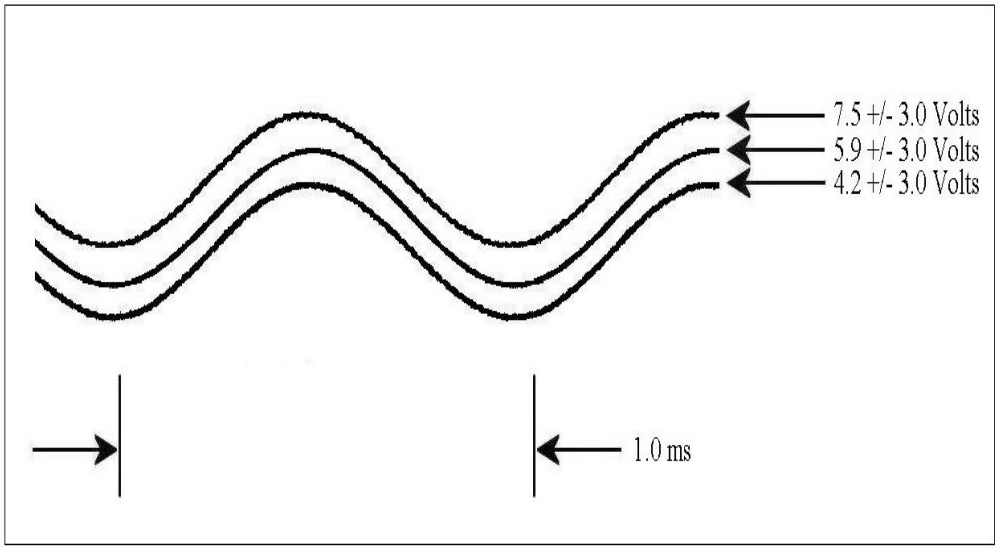

Fig. 21: One kHz Output and Tracking Rails

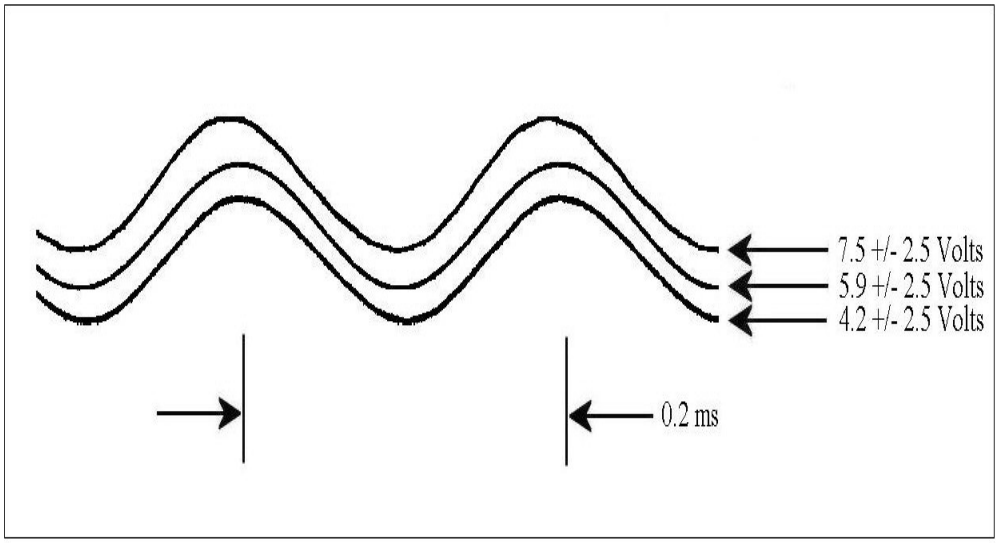

Fig. 22: 5 kHz Sinusoid Output and Tracking Rails

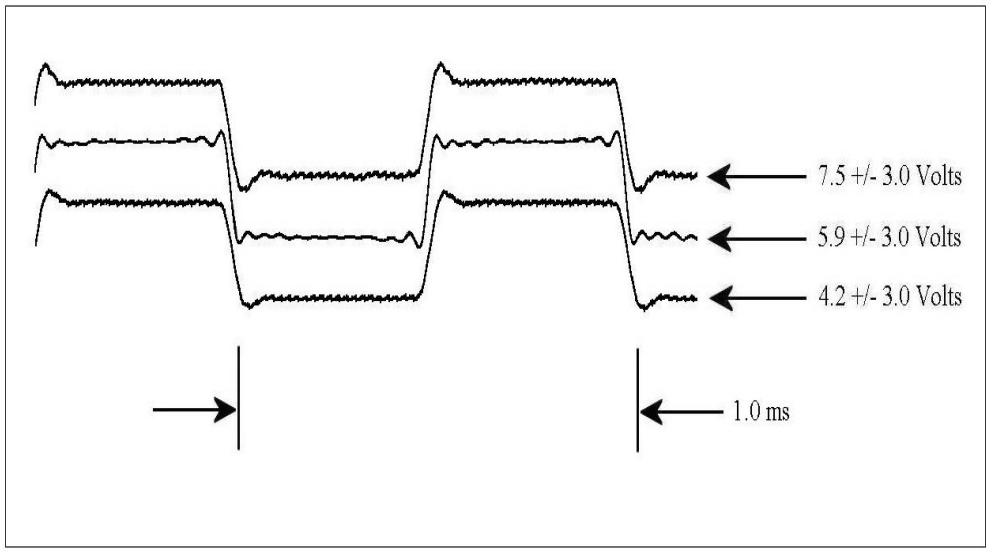

Fig. 23: 1 kHz Square Wave Output and Tracking Rails